



# ILI9163C

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## **a-Si TFT LCD Single Chip Driver 132RGBx162 Resolution and 262K color**

### **Specification** ***Preliminary***

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## 1. Introduction

ILI9163C is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 132RGBx162 dots, comprising a 396-channel source driver, a 162-channel gate driver, 48,114bytes GRAM for graphic data of 132RGBx162 dots, and power supply circuit.

The ILI9163C supports 18-/16-/9-/8-bit data bus interface and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

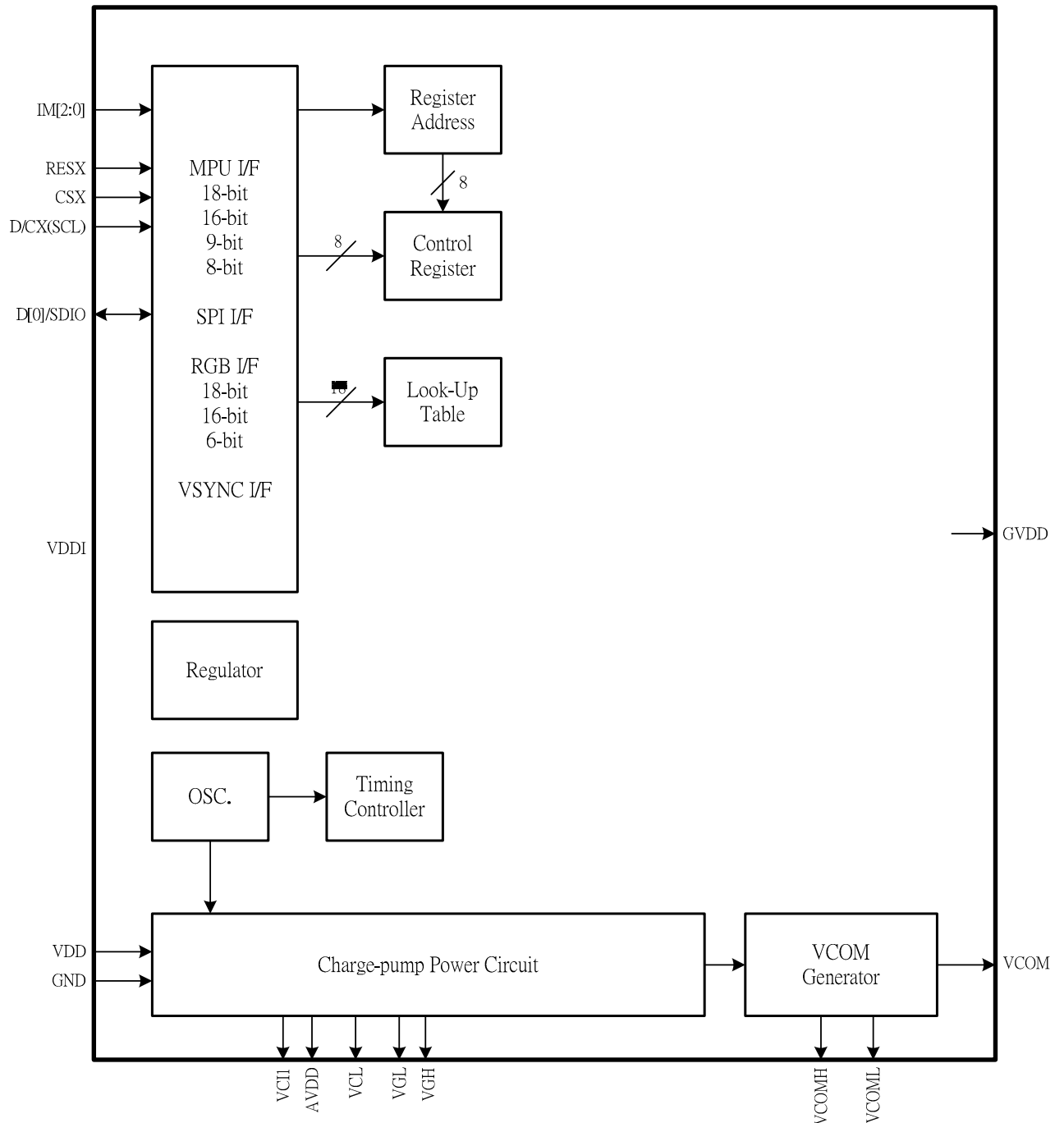
ILI9163C can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9163C also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9163C an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

## 2. Features

- ◆ Display resolution: [132xRGB](H) x 162(V)
- ◆ Output:
  - 396 source outputs
  - 162 gate outputs
  - Common electrode output
- ◆ AM-LCD driver with on-chip full display RAM: 48,114 bytes
- ◆ MCU Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 6800-series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-pin/4-pin serial interface
- ◆ Display mode:
  - Full color mode (idle mode off): 262K-colors
  - Reduced color mode (idle mode on): 8-colors (3-bits MSB bits mode)
- ◆ On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - 8 preset gamma curve selectable
  - Line/frame inversion
  - MTP to store initialization register setting
  - Factory default value(Contrast, Module ID, Module version, etc) are stored on the display module

- ◆ MTP:
  - 7-bits for ID2
  - 8-bits for ID3
  - 7-bits for VCOM adjustment
- ◆ Low –power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3 V (interface I/O)
    - VPNL = 2.5V ~ 4.8 V (analog)
- ◆ LCD Voltage drive:
  - Source/VCOM power supply voltage
    - AVDD – GND = 4.5V ~ 6.0
    - VCL – GND = -1.0V ~ -3.0V
    - VDD – VCL  $\leq$  6.0V
  - Gate driver output voltage
    - VGH – GND = 10V ~ 16V
    - VGL – GND = -9V ~ -16V
    - VGH – VGL  $\leq$  30V
  - VCOM driver output voltage
    - VCOMH = 2.5V ~5V
    - VCOML = -2.5V ~ 0V
    - VCOMH-VCOML  $\leq$  6.0V
- ◆ Operate temperature range: -40°C to 85°C

### 3. Block Diagram



## 4. Pin Descriptions

Pin Name	I/O	Descriptions															
P68	I	8080/6800 MCU Interface mode selection.  P68='1': select 6800-MCU parallel interface P68='0': select 8080-MCU parallel interface  If not used, please fix this pin at GND level.															
IM2	I	MCU Parallel interface bus and Serial interface select - IM2='1';Parallel Interface - IM2='0';Serial Interface															
IM1, IM0	I	MCU parallel interface type selection <table border="1"> <thead> <tr> <th>IM1</th><th>IM0</th><th>Parallel interface</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>MCU 8-bit Parallel</td></tr> <tr> <td>0</td><td>1</td><td>MCU 16-bit Parallel</td></tr> <tr> <td>1</td><td>0</td><td>MCU 9-bit Parallel</td></tr> <tr> <td>1</td><td>1</td><td>MCU 18-bit Parallel</td></tr> </tbody> </table>	IM1	IM0	Parallel interface	0	0	MCU 8-bit Parallel	0	1	MCU 16-bit Parallel	1	0	MCU 9-bit Parallel	1	1	MCU 18-bit Parallel
IM1	IM0	Parallel interface															
0	0	MCU 8-bit Parallel															
0	1	MCU 16-bit Parallel															
1	0	MCU 9-bit Parallel															
1	1	MCU 18-bit Parallel															
SPI4W	I	SPI interface selection pin SPI4W='0': 3-wire SPI. (default) SPI4W='1': 4-wire SPI. This pin is internal pull low.															
RESX	I	Chip reset pin ("Low Active"). This signal low will reset the device and must be applied to properly initialize the chip.															
CSX	I	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MCU interface mode only.															
D/CX (SCL)	I	Display data / Command selection pin in parallel and SCL in 3-pin SPI interface. D/CX='1': Display data. D/CX='0': Command data. If not used, please connect this pin to GND.															
RDX (E)	I	Read enable in 8080-parallel interface and Read/ Write operation enable pin in 6800-parallel interface. In 8080-parallel interface, if not used, please connect this pin to VDDI. In 6800-parallel interface, if not used, please connect this pin to VDDI or GND.															
WRX (R/Wx)(D/CX)	I	Write enable in parallel interface. WRX: for 8080 MCU R/WX: for 6800 MCU D/CX: for 4-wire SPI If not used, please connect this pin to VDDI or GND.															
D[17:1] D[0]/SDIO	I/O	When RCM='0' (MCU I/F), D[17:0] are used to MCU parallel interface data bus, and D0 is also the serial input/ output signal in SPI interface mode. In serial interface, D[17:1] are not used and should be connected to ground.															
TE	O	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W															

Pin Name	I/O	Descriptions																												
		command. When this pin is not activated, this pin is low. If not used, please open this pin.																												
SDA	I/O	Serial data input / output and applied on the rising edge of the SCL signal, when RCM[1:0]= '0X' (MCU I/F) -If it's not used, please fix this pin at GND level.																												
PCLK	I	Pixel clock signal in RGB I/F mode. -If it's not used, please fix this pin at GND level.																												
VS	I	Vertical sync. Signal in RGB I/F mode. -If it's not used, please fix this pin at GND level.																												
HS	I	Horizontal sync. Signal in RGB I/F mode. -If it's not used, please fix this pin at GND level.																												
DE	I	Data enable signal in RGB I/F mode. -If it's not used, please fix this pin at GND level.																												
OSC	O	Oscillator output or test purpose.																												
EXTC	I	To use extended command set, please connect this pin to VDDI. During normal operation, please open this pin. (It has an internal pull low resistor.) EXTC='1', all the command can be used. EXTC='0', only Command (00h~3Ah, DAh~DCh) can be used																												
IDM	I	Normal mode and Idle mode control pin <table><tr><th>IDM</th><th>Idle mode H/W controller</th></tr><tr><td>0</td><td>Normal display (can be changed to Idle mode by S/W)</td></tr><tr><td>1</td><td>Idle mode</td></tr></table>	IDM	Idle mode H/W controller	0	Normal display (can be changed to Idle mode by S/W)	1	Idle mode																						
IDM	Idle mode H/W controller																													
0	Normal display (can be changed to Idle mode by S/W)																													
1	Idle mode																													
GM2,GM1,GM0	I	Panel Resolution selection pins <table><tr><th>GM2</th><th>GM1</th><th>GM0</th><th>Resolution selection</th></tr><tr><td>0</td><td>0</td><td>0</td><td>132RGB x 162(S1~396 and G1~ G162 output)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>128RGB x 128(S7~390 and G2~ G129 output)</td></tr><tr><td>0</td><td>1</td><td>0</td><td>120RGB x 160(S7~366 and G2~ G161 output)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>128RGB x 160(S7~390 and G2~ G161 output)</td></tr><tr><td>1</td><td>0</td><td>0</td><td>130RGB x 130(S7~396 and G2~ G131 output)</td></tr><tr><td>1</td><td>0</td><td>1</td><td>132RGB x 132(S1~396 and G2~ G133 output)</td></tr></table>	GM2	GM1	GM0	Resolution selection	0	0	0	132RGB x 162(S1~396 and G1~ G162 output)	0	0	1	128RGB x 128(S7~390 and G2~ G129 output)	0	1	0	120RGB x 160(S7~366 and G2~ G161 output)	0	1	1	128RGB x 160(S7~390 and G2~ G161 output)	1	0	0	130RGB x 130(S7~396 and G2~ G131 output)	1	0	1	132RGB x 132(S1~396 and G2~ G133 output)
GM2	GM1	GM0	Resolution selection																											
0	0	0	132RGB x 162(S1~396 and G1~ G162 output)																											
0	0	1	128RGB x 128(S7~390 and G2~ G129 output)																											
0	1	0	120RGB x 160(S7~366 and G2~ G161 output)																											
0	1	1	128RGB x 160(S7~390 and G2~ G161 output)																											
1	0	0	130RGB x 130(S7~396 and G2~ G131 output)																											
1	0	1	132RGB x 132(S1~396 and G2~ G133 output)																											
RCM[1:0]	I	RGB and MCU interface mode selection pin <table><tr><th>RCM1</th><th>RCM0</th><th>Resolution selection</th></tr><tr><td>0</td><td>0</td><td>MCU interface mode</td></tr><tr><td>0</td><td>1</td><td>MCU interface mode</td></tr><tr><td>1</td><td>0</td><td>RGB interface(1)</td></tr><tr><td>1</td><td>1</td><td>RGB interface(2)</td></tr></table>	RCM1	RCM0	Resolution selection	0	0	MCU interface mode	0	1	MCU interface mode	1	0	RGB interface(1)	1	1	RGB interface(2)													
RCM1	RCM0	Resolution selection																												
0	0	MCU interface mode																												
0	1	MCU interface mode																												
1	0	RGB interface(1)																												
1	1	RGB interface(2)																												
SRGB	I	RGB direction select H/W pin for Color filter default setting. <table><tr><th>SRGB</th><th>Color mapping selection</th></tr><tr><td>0</td><td>S1, S2, S3 filter order = 'R', 'G', 'B'</td></tr><tr><td>1</td><td>S1, S2, S3 filter order = 'B', 'G', 'R'</td></tr></table> If the register is not changed, this H/W pin is always valid. If the register be changed, should be following registers setting. When Power On or H/W reset, this function follow H/W pins setting first.	SRGB	Color mapping selection	0	S1, S2, S3 filter order = 'R', 'G', 'B'	1	S1, S2, S3 filter order = 'B', 'G', 'R'																						
SRGB	Color mapping selection																													
0	S1, S2, S3 filter order = 'R', 'G', 'B'																													
1	S1, S2, S3 filter order = 'B', 'G', 'R'																													
SMX	I	Source output direction H/W select pin																												

Pin Name	I/O	Descriptions																											
		<table><tr><th rowspan="2">SMX</th><th colspan="6">Source Output Direction</th></tr><tr><th>GM='101'</th><th>GM='100'</th><th>GM='011'</th><th>GM='010'</th><th>GM='001'</th><th>GM='000'</th></tr><tr><td>0</td><td>S1 → S396</td><td>S7 → S396</td><td>S7 → S390</td><td>S7 → S366</td><td>S7 → S390</td><td>S1 → S396</td></tr><tr><td>1</td><td>S396 → S1</td><td>S396 → S7</td><td>S390 → S7</td><td>S366 → S7</td><td>S390 → S7</td><td>S396 → S1</td></tr></table> <p>If the register is not changed, this H/W pin is always valid. If the register be changed, should be following registers setting. When Power On or H/W reset, this function follow H/W pins setting first.</p>	SMX	Source Output Direction						GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'	0	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396	1	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1
SMX	Source Output Direction																												
	GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'																							
0	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396																							
1	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1																							
SMY	I	<p>Gate output direction H/W select pin</p> <table><tr><th rowspan="2">SMY</th><th colspan="5">Gate Output Direction</th></tr><tr><th>GM='101'</th><th>GM='100'</th><th>GM='011', '010'</th><th>GM='001'</th><th>GM='000'</th></tr><tr><td>0</td><td>G2 → G133</td><td>G2 → G131</td><td>G2 → G161</td><td>G2 → G129</td><td>G1 → G162</td></tr><tr><td>1</td><td>G133 → G2</td><td>G131 → G2</td><td>G161 → G2</td><td>G129 → G2</td><td>G162 → G1</td></tr></table> <p>If the register is not changed, this H/W pin is always valid. If the register be changed, should be following registers setting. When Power On or H/W reset, this function follow H/W pins setting first.</p>	SMY	Gate Output Direction					GM='101'	GM='100'	GM='011', '010'	GM='001'	GM='000'	0	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162	1	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1				
SMY	Gate Output Direction																												
	GM='101'	GM='100'	GM='011', '010'	GM='001'	GM='000'																								
0	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162																								
1	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1																								
SHUT	I	<p>Display On/ Off H/W control pin In RGB I/F</p> <table><tr><th>SHUT</th><th>Display On/Off in RGB interface</th></tr><tr><td>0</td><td>Display on</td></tr><tr><td>1</td><td>Display off</td></tr></table> <p>Please refer RGB I/F for detail using.</p>	SHUT	Display On/Off in RGB interface	0	Display on	1	Display off																					
SHUT	Display On/Off in RGB interface																												
0	Display on																												
1	Display off																												
REV	I	<p>Source output data polarity select H/W pin.</p> <table><tr><th>REV</th><th>Source output data polarity</th></tr><tr><td>0</td><td>Data not reverse</td></tr><tr><td>1</td><td>Data reverse</td></tr></table> <p>If the register is not changed, this H/W pin is always valid. If the register be changed, should be following registers setting. When Power On or H/W reset, this function follow H/W pins setting first.</p>	REV	Source output data polarity	0	Data not reverse	1	Data reverse																					
REV	Source output data polarity																												
0	Data not reverse																												
1	Data reverse																												
GS	I	<p>Input pin to select the gamma curve order</p> <p>Connect to VDDI for GC0(2,0), GC1(1.8), GC2(2.5), GC3(1.0)</p> <p>Connect to GND for GC0(1,0), GC1(2.5), GC2(2.2), GC3(1.8)</p>																											
TESEL	I	<p>There is a pull-high resistor in the pin.</p> <p>This pin is only for GM[2:0]='000' mode</p> <p>Connect to VDDI (Disable scroll function)</p> <p>Connect to GND (Enable scroll function)</p>																											
RL	I	<p>Source output direction H/W select pin in RGB I/F Mode 2</p> <p>When SMX=0</p> <table><tr><th rowspan="2">RL</th><th colspan="6">Module source output direction</th></tr><tr><th>GM='101'</th><th>GM='100'</th><th>GM='011'</th><th>GM='010'</th><th>GM='001'</th><th>GM='000'</th></tr><tr><td>0</td><td>S1 → S396</td><td>S7 → S396</td><td>S7 → S390</td><td>S7 → S366</td><td>S7 → S390</td><td>S1 → S396</td></tr><tr><td>1</td><td>S396 → S1</td><td>S396 → S7</td><td>S390 → S7</td><td>S366 → S7</td><td>S390 → S7</td><td>S396 → S1</td></tr></table>	RL	Module source output direction						GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'	0	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396	1	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1
RL	Module source output direction																												
	GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'																							
0	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396																							
1	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1																							

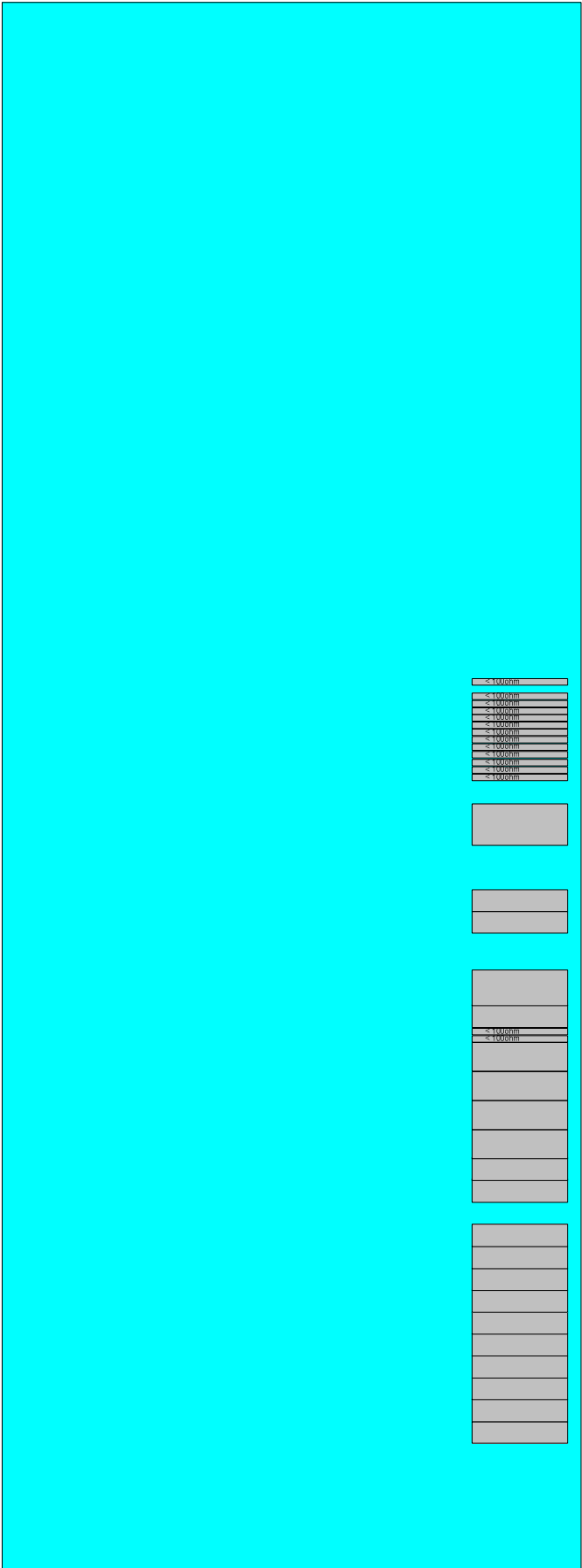
Pin Name	I/O	Descriptions																																														
		<div>When SMX=1</div> <table><tr><th rowspan="2">RL</th><th colspan="6">Module source output direction</th></tr><tr><th>GM='101'</th><th>GM='100'</th><th>GM='011'</th><th>GM='010'</th><th>GM='001'</th><th>GM='000'</th></tr><tr><td>0</td><td>S396 → S1</td><td>S396 → S7</td><td>S390 → S7</td><td>S366 → S7</td><td>S390 → S7</td><td>S396 → S1</td></tr><tr><td>1</td><td>S1 → S396</td><td>S7 → S396</td><td>S7 → S390</td><td>S7 → S366</td><td>S7 → S390</td><td>S1 → S396</td></tr></table>	RL	Module source output direction						GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'	0	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1	1	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396																			
RL	Module source output direction																																															
	GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'																																										
0	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1																																										
1	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396																																										
TB	I	<div>Gate output direction H/W select pin on RGB I/F Mode 2.</div> <div>When SMY=0</div> <table><tr><th rowspan="2">TB</th><th colspan="5">Module gate output direction</th></tr><tr><th>GM='101'</th><th>GM='100'</th><th>GM='011', 010'</th><th>GM='001'</th><th>GM='000'</th></tr><tr><td>0</td><td>G2 → G133</td><td>G2 → G131</td><td>G2 → G161</td><td>G2 → G129</td><td>G1 → G162</td></tr><tr><td>1</td><td>G133 → G2</td><td>G131 → G2</td><td>G161 → G2</td><td>G129 → G2</td><td>G162 → G1</td></tr></table> <div>When SMY=1</div> <table><tr><th rowspan="2">TB</th><th colspan="5">Module gate output direction</th></tr><tr><th>GM='101'</th><th>GM='100'</th><th>GM='011', 010'</th><th>GM='001'</th><th>GM='000'</th></tr><tr><td>0</td><td>G133 → G2</td><td>G131 → G2</td><td>G161 → G2</td><td>G129 → G2</td><td>G162 → G1</td></tr><tr><td>1</td><td>G2 → G133</td><td>G2 → G131</td><td>G2 → G161</td><td>G2 → G129</td><td>G1 → G162</td></tr></table> <div>Please refer RGB I/F detail using</div>	TB	Module gate output direction					GM='101'	GM='100'	GM='011', 010'	GM='001'	GM='000'	0	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162	1	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1	TB	Module gate output direction					GM='101'	GM='100'	GM='011', 010'	GM='001'	GM='000'	0	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1	1	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162
TB	Module gate output direction																																															
	GM='101'	GM='100'	GM='011', 010'	GM='001'	GM='000'																																											
0	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162																																											
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0	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1																																											
1	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162																																											
S1 ~ S396	O	Source driver output pins.																																														
G1 ~ G162	O	Gate driver output pins.																																														
VPNL	P	Power supply for analog circuit. Could connect to external power supply (VPNL=2.5~4.8V).																																														
VDDI	P	Power supply for interface logic circuits (1.65 ~ 3.3 V)																																														
VCC	P	Power supply for internal logic regulator.																																														
GND	P	GND voltage output level for control pins.																																														
VDDIO	P	VDDI voltage output level for control pins using.																																														
GNDO	P	GND voltage output level for control pins using.																																														
VCI1	I/O	A reference voltage in step-up circuit 1 Connect a capacitor for stabilization																																														
AVDD	P	A power output pin for source driver block that is generated from power block. Output of booster 1 circuit (output of 2-times output of VCI1) Connect a capacitor for stabilization.																																														
VCL	P	A power supply pin for generating VCOML Connect a capacitor for stabilization																																														
GVDD	P	A standard level for grayscale voltage generator. Connect a capacitor for stabilization.																																														
VGH	P	Positive power supply for the gate driver. Connect a capacitor for stabilization																																														
VGL	P	Negative power supply for the gate driver. Connect a capacitor for stabilization																																														
VCL	P	Power supply to drive VCOML. Connect a capacitor for stabilization																																														

Pin Name	I/O	Descriptions
VCOM	O	TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML. Registers set the alternating cycle for operating or halting VCOM.
VCOMH	O	The high level of VCOM AC voltage.
VCOML	O	The low level of VCOM AC voltage.
TESTOSC	I	These test pins for Driver vender test used. Please open these pins or fix to GND.
TESTDA[6:0]	O	These test pins for Driver vendor test used. Please open these pins.
DUMMYR1-DUMMYR2	-	DUMMYR1 and DUMMYR2 are short-circuited within the chip for COG contact resistance measurement. Please leave them open when not used.
DUMMY1-DUMMY18 DUMMY	-	Dummy pins. During normal operation, leave these pads open.

**Liquid crystal power supply specifications Table 1**

No.	Item	Description
1	TFT Source Driver	396 pins (132 x RGB)
2	TFT Gate Driver	162 pins
3	TFT Display's Capacitor Structure	Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S396 V0 ~ V63 grayscales
		G1 ~ G162 VGH – VGL
		VCOM VCOMH – VCOML: Amplitude = electronic volumes
5	Input Voltage	VDDI 1.65 ~ 3.30V
		VPNL 2.50 ~ 4.80V
6	Liquid Crystal Drive Voltages	AVDD 4.5V ~ 6.0V
		VGH 10V ~ 16V
		VGL -9V ~ -16V
		VCL -1.7V ~ -2.7V
		VGH – VGL Max. 30V
		VPNL – VCL Max. 6.0V
	Internal Step-up Circuits	AVDD VCI x2
		VGH VCI1 x4, x5, x6
		VGL VCI -x5, -x6
		VCL VCI x-1



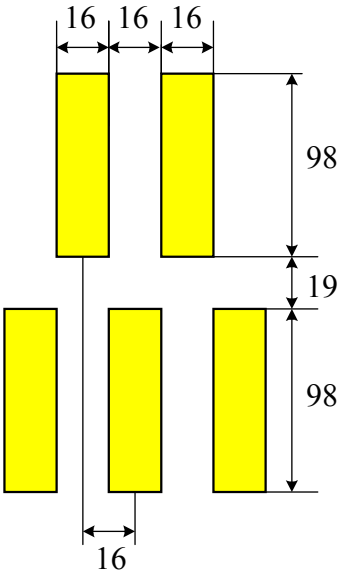


No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	Dummy1	-4750	-238.5	61	AGND	-1750	-238.5	121	AVDD	1550	-238.5	181	VCOML	4550	-238.5	241	G56	3892	227
2	VDDIO	-4700	-238.5	62	AGND	-1700	-238.5	122	AVDD	1600	-238.5	182	VCOM	4600	-238.5	242	G54	3876	110
3	EXTC	-4650	-238.5	63	RDX	-1630	-238.5	123	AVDD	1650	-238.5	183	VCOM	4650	-238.5	243	G52	3860	227
4	GNDO	-4600	-238.5	64	D/CX	-1570	-238.5	124	AVDD	1700	-238.5	184	VCOM	4700	-238.5	244	G50	3844	110
5	IM0	-4550	-238.5	65	TESEL	-1510	-238.5	125	GVDD	1750	-238.5	185	DUMMY2	4750	-238.5	245	G48	3828	227
6	VDDIO	-4500	-238.5	66	GNDO	-1450	-238.5	126	GVDD	1800	-238.5	186	DUMMY3	4772	110	246	G46	3812	110
7	IM1	-4450	-238.5	67	D17	-1390	-238.5	127	GVDD	1850	-238.5	187	DUMMY4	4756	227	247	G44	3796	227
8	GNDO	-4400	-238.5	68	D16	-1330	-238.5	128	DUMMYR1	1900	-238.5	188	G162	4740	110	248	G42	3780	110
9	P68	-4350	-238.5	69	D15	-1270	-238.5	129	DUMMYR2	1950	-238.5	189	G160	4724	227	249	G40	3764	227
10	VDDIO	-4300	-238.5	70	D14	-1210	-238.5	130	Dummy	2000	-238.5	190	G158	4708	110	250	G38	3748	110
11	RCM0	-4250	-238.5	71	D13	-1150	-238.5	131	Dummy	2050	-238.5	191	G156	4692	227	251	G36	3732	227
12	GNDO	-4200	-238.5	72	D12	-1090	-238.5	132	Dummy	2100	-238.5	192	G154	4676	110	252	G34	3716	110
13	RCM1	-4150	-238.5	73	D11	-1030	-238.5	133	Dummy	2150	-238.5	193	G152	4660	227	253	G32	3700	227
14	VDDIO	-4100	-238.5	74	D10	-970	-238.5	134	Dummy	2200	-238.5	194	G150	4644	110	254	G30	3684	110
15	SRGB	-4050	-238.5	75	D9	-910	-238.5	135	Dummy	2250	-238.5	195	G148	4628	227	255	G28	3668	227
16	GNDO	-4000	-238.5	76	D8	-850	-238.5	136	Dummy	2300	-238.5	196	G146	4612	110	256	G26	3652	110
17	SMX	-3950	-238.5	77	D1	-790	-238.5	137	Dummy	2350	-238.5	197	G144	4596	227	257	G24	3636	227
18	VDDIO	-3900	-238.5	78	D3	-730	-238.5	138	Dummy	2400	-238.5	198	G142	4580	110	258	G22	3620	110
19	SMY	-3850	-238.5	79	D5	-670	-238.5	139	Dummy	2450	-238.5	199	G140	4564	227	259	G20	3604	227
20	GNDO	-3800	-238.5	80	D7	-610	-238.5	140	Dummy	2500	-238.5	200	G138	4548	110	260	G18	3588	110
21	IDM	-3750	-238.5	81	TE	-550	-238.5	141	Dummy	2550	-238.5	201	G136	4532	227	261	G16	3572	227
22	VDDIO	-3700	-238.5	82	RESX	-490	-238.5	142	Dummy	2600	-238.5	202	G134	4516	110	262	G14	3556	110
23	REV	-3650	-238.5	83	CSX	-430	-238.5	143	Dummy	2650	-238.5	203	G132	4500	227	263	G12	3540	227
24	GNDO	-3600	-238.5	84	D6	-370	-238.5	144	Dummy	2700	-238.5	204	G130	4484	110	264	G10	3524	110
25	RL	-3550	-238.5	85	D4	-310	-238.5	145	Dummy	2750	-238.5	205	G128	4468	227	265	G8	3508	227
26	VDDIO	-3500	-238.5	86	D2	-250	-238.5	146	AGND	2800	-238.5	206	G126	4452	110	266	G6	3492	110
27	TB	-3450	-238.5	87	IM2	-190	-238.5	147	AGND	2850	-238.5	207	G124	4436	227	267	G4	3476	227
28	GNDO	-3400	-238.5	88	D0	-130	-238.5	148	AGND	2900	-238.5	208	G122	4420	110	268	G2	3460	110
29	SHUT	-3350	-238.5	89	WRX	-70	-238.5	149	VCL	2950	-238.5	209	G120	4404	227	269	DUMMY5	3444	227
30	VDDIO	-3300	-238.5	90	PCLK	0	-238.5	150	VCL	3000	-238.5	210	G118	4388	110	270	DUMMY6	3428	110
31	LCM0	-3250	-238.5	91	DE	50	-238.5	151	VCL	3050	-238.5	211	G116	4372	227	271	DUMMY7	3412	227
32	GNDO	-3200	-238.5	92	HS	100	-238.5	152	Dummy	3100	-238.5	212	G114	4356	110	272	DUMMY8	3396	110
33	LCM1	-3150	-238.5	93	VS	150	-238.5	153	Dummy	3150	-238.5	213	G112	4340	227	273	S396	3380	227
34	VDDIO	-3100	-238.5	94	TEST_IN[2]	200	-238.5	154	Dummy	3200	-238.5	214	G110	4324	110	274	S395	3364	110
35	GM2	-3050	-238.5	95	TEST_IN[1]	250	-238.5	155	Dummy	3250	-238.5	215	G108	4308	227	275	S394	3348	227
36	GNDO	-3000	-238.5	96	TEST_IN[0]	300	-238.5	156	Dummy	3300	-238.5	216	G106	4292	110	276	S393	3332	110
37	GM1	-2950	-238.5	97	DGND	350	-238.5	157	Dummy	3350	-238.5	217	G104	4276	227	277	S392	3316	227
38	VDDIO	-2900	-238.5	98	DGND	400	-238.5	158	Dummy	3400	-238.5	218	G102	4260	110	278	S391	3300	110
39	GM0	-2850	-238.5	99	DGND	450	-238.5	159	Dummy	3450	-238.5	219	G100	4244	227	279	S390	3284	227
40	GNDO	-2800	-238.5	100	DGND	500	-238.5	160	Dummy	3500	-238.5	220	G98	4228	110	280	S389	3268	110
41	SDA	-2750	-238.5	101	DGND	550	-238.5	161	Dummy	3550	-238.5	221	G96	4212	227	281	S388	3252	227
42	GS	-2700	-238.5	102	DGND	600	-238.5	162	Dummy	3600	-238.5	222	G94	4196	110	282	S387	3236	110
43	SPI4W	-2650	-238.5	103	VDDI	650	-238.5	163	Dummy	3650	-238.5	223	G92	4180	227	283	S386	3220	227
44	VDDIO	-2600	-238.5	104	VDDI	700	-238.5	164	Dummy	3700	-238.5	224	G90	4164	110	284	S385	3204	110
45	TESTMODE[2]	-2550	-238.5	105	VDDI	750	-238.5	165	Dummy	3750	-238.5	225	G88	4148	227	285	S384	3188	227
46	TEST_IN[5]	-2500	-238.5	106	VDDI	800	-238.5	166	Dummy	3800	-238.5	226	G86	4132	110	286	S383	3172	110
47	TEST_IN[4]	-2450	-238.5	107	VDDI	850	-238.5	167	Dummy	3850	-238.5	227	G84	4116	227	287	S382	3156	227
48	TEST_IN[3]	-2400	-238.5	108	VDDI	900	-238.5	168	Dummy	3900	-238.5	228	G82	4100	110	288	S381	3140	110
49	TESTOSC	-2350	-238.5	109	VCC	950	-238.5	169	Dummy	3950	-238.5	229	G80	4084	227	289	S380	3124	227
50	OSC	-2300	-238.5	110	VCC	1000	-238.5	170	VGL	4000	-238.5	230	G78	4068	110	290	S379	3108	110
51	VPNL	-2250	-238.5	111	VCC	1050	-238.5	171	VGL	4050	-238.5	231	G76	4052	227	291	S378	3092	227
52	VPNL	-2200	-238.5	112	VCI1	1100	-238.5	172	VGL	4100	-238.5	232	G74	4036	110	292	S377	3076	110
53	VPNL	-2150	-238.5	113	VCI1	1150	-238.5	173	VGH	4150	-238.5	233	G72	4020	227	293	S376	3060	227
54	VPNL	-2100	-238.5	114	VCI1	1200	-238.5	174	VGH	4200	-238.5	234	G70	4004	110	294	S375	3044	110
55	VPNL	-2050	-238.5	115	Dummy	1250	-238.5	175	VGH	4250	-238.5	235	G68	3988	227	295	S374	3028	227
56	VPNL	-2000	-238.5	116	Dummy	1300	-238.5	176	VCOMH	4300	-238.5	236	G66	3972	110	296	S373	3012	110
57	AGND	-1950	-238.5	117	Dummy	1350	-238.5	177	VCOMH	4350	-238.5	237	G64	3956	227	297	S372	2996	227
58	AGND	-1900	-238.5	118	TEST_MODE[0]	1400	-238.5	178	VCOMH	4400	-238.5	238	G62	3940	110	298	S371	2980	110
59	AGND	-1850	-238.5	119	TEST_MODE[1]	1450	-238.5	179	VCOML	4450	-238.5	239	G60	3924	227	299	S370	2964	227
60	AGND	-1800	-238.5	120	AVDD	1500	-238.5	180	VCOML	4500	-238.5	240	G58	3908	110	300	S369	2948	110

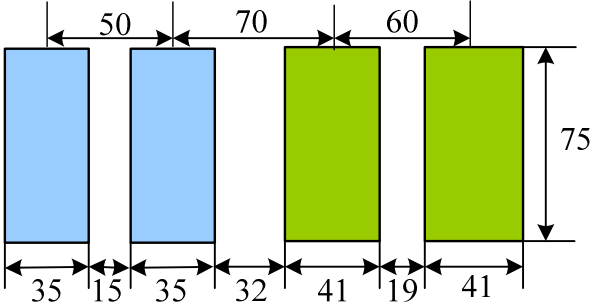
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
301	S368	2932	227	361	S308	1972	227	421	S248	1012	227	481	S192	-324	110
302	S367	2916	110	362	S307	1956	110	422	S247	996	110	482	S191	-340	227
303	S366	2900	227	363	S306	1940	227	423	S246	980	227	483	S190	-356	110
304	S365	2884	110	364	S305	1924	110	424	S245	964	110	484	S189	-372	227
305	S364	2868	227	365	S304	1908	227	425	S244	948	227	485	S188	-388	110
306	S363	2852	110	366	S303	1892	110	426	S243	932	110	486	S187	-404	227
307	S362	2836	227	367	S302	1876	227	427	S242	916	227	487	S186	-420	110
308	S361	2820	110	368	S301	1860	110					541	S132	-1284	110
												542	S131	-1300	227
												543	S130	-1316	110
												544	S129	-1332	227
												545	S128	-1348	110
												546	S127	-1364	227
												547	S126	-1380	110

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
601	S72	-2244	110	661	S12	-3204	110	721	G89	-4164	110
602	S71	-2260	227	662	S11	-3220	227	722	G91	-4180	227
603	S70	-2276	110	663	S10	-3236	110	723	G93	-4196	110
604	S69	-2292	227	664	S9	-3252	227	724	G95	-4212	227
605	S68	-2308	110	665	S8	-3268	110	725	G97	-4228	110
606	S67	-2324	227	666	S7	-3284	227	726	G99	-4244	227
607	S66	-2340	110	667	S6	-3300	110	727	G101	-4260	110
608	S65	-2356	227	668	S5	-3316	227	728	G103	-4276	227
609	S64	-2372	110	669	S4	-3332	110	729	G105	-4292	110
610	S63	-2388	227	670	S3	-3348	227	730	G107	-4308	227
611	S62	-2404	110	671	S2	-3364	110	731	G109	-4324	110
612	S61	-2420	227	672	S1	-3380	227	732	G111	-4340	227
613	S60	-2436	110	673	Dummy13	-3396	110	733	G113	-4356	110
614	S59	-2452	227	674	Dummy14	-3412	227	734	G115	-4372	227
615	S58	-2468	110	675	Dummy15	-3428	110	735	G117	-4388	110
616	S57	-2484	227	676	Dummy16	-3444	227	736	G119	-4404	227
617	S56	-2500	110	677	G1	-3460	110	737	G121	-4420	110
618	S55	-2516	227	678	G3	-3476	227	738	G123	-4436	227
619	S54	-2532	110	679	G5	-3492	110	739	G125	-4452	110
620	S53	-2548	227	680	G7	-3508	227	740	G127	-4468	227
621	S52	-2564	110	681	G9	-3524	110	741	G129	-4484	110
622	S51	-2580	227	682	G11	-3540	227	742	G131	-4500	227
623	S50	-2596	110	683	G13	-3556	110	743	G133	-4516	110
624	S49	-2612	227	684	G15	-3572	227	744	G135	-4532	227
625	S48	-2628	110	685	G17	-3588	110	745	G137	-4548	110
626	S47	-2644	227	686	G19	-3604	227	746	G139	-4564	227
627	S46	-2660	110	687	G21	-3620	110	747	G141	-4580	110
628	S45	-2676	227	688	G23	-3636	227	748	G143	-4596	227
629	S44	-2692	110	689	G25	-3652	110	749	G145	-4612	110
630	S43	-2708	227	690	G27	-3668	227	750	G147	-4628	227
631	S42	-2724	110	691	G29	-3684	110	751	G149	-4644	110
632	S41	-2740	227	692	G31	-3700	227	752	G151	-4660	227
633	S40	-2756	110	693	G33	-3716	110	753	G153	-4676	110
634	S39	-2772	227	694	G35	-3732	227	754	G155	-4692	227
635	S38	-2788	110	695	G37	-3748	110	755	G157	-4708	110
636	S37	-2804	227	696	G39	-3764	227	756	G159	-4724	227
637	S36	-2820	110	697	G41	-3780	110	757	G161	-4740	110
638	S35	-2836	227	698	G43	-3796	227	758	Dummy17	-4756	227
639	S34	-2852	110	699	G45	-3812	110	759	Dummy18	-4772	110
640	S33	-2868	227	700	G47	-3828	227				
641	S32	-2884	110	701	G49	-3844	110		ALK-R	4841	-220
642	S31	-2900	227	702	G51	-3860	227		ALK-L	-4841	-220
643	S30	-2916	110	703	G53	-3876	110				
644	S29	-2932	227	704	G55	-3892	227				
645	S28	-2948	110	705	G57	-3908	110				
646	S27	-2964	227	706	G59	-3924	227				
647	S26	-2980	110	707	G61	-3940	110				
648	S25	-2996	227	708	G63	-3956	227				
649	S24	-3012	110	709	G65	-3972	110				
650	S23	-3028	227	710	G67	-3988	227				
651	S22	-3044	110	711	G69	-4004	110				
652	S21	-3060	227	712	G71	-4020	227				
653	S20	-3076	110	713	G73	-4036	110				
654	S19	-3092	227	714	G75	-4052	227				
655	S18	-3108	110	715	G77	-4068	110				
656	S17	-3124	227	716	G79	-4084	227				
657	S16	-3140	110	717	G81	-4100	110				
658	S15	-3156	227	718	G83	-4116	227				
659	S14	-3172	110	719	G85	-4132	110				
660	S13	-3188	227	720	G87	-4148	227				

S1 ~ S396  
G1 ~ G162



Input Pad



## 6. Function Description

### 6.1 MCU Interface Type Selection

The selection of a given interfaces are done by setting P68, IM2, IM1, and IM0 pins as show in below tables.

**Table 6.1.1 MCU Interface Type Selection**

P68	IM2	IM1	IM0	Interface	Read back selection
-	0	-	-	Serial interface	Via the read instruction (12-bit, 16-bit and 18-bit read parameter)
0	1	0	0	8080 MCU 8-bit Parallel	RDX strobe(8-bit read data and 8-bit read parameter)
0	1	0	1	8080 MCU 16-bit Parallel	RDX strobe(16-bit read data and 8-bit read parameter)
0	1	1	0	8080 MCU 9-bit Parallel	RDX strobe(9-bit read data and 8-bit read parameter)
0	1	1	1	8080 MCU 18-bit Parallel	RDX strobe(18-bit read data and 8-bit read parameter)
-	0	-	-	Serial interface	Via the read instruction (12-bit, 16-bit and 19-bit read parameter)
1	1	0	0	6800 MCU 8-bit Parallel	E strobe(8-bit read data and 8-bit read parameter)
1	1	0	1	6800 MCU 16-bit Parallel	E strobe(9-bit read data and 8-bit read parameter)
1	1	1	0	6800 MCU 9-bit Parallel	E strobe(16-bit read data and 8-bit read parameter)
1	1	1	1	6800 MCU 18-bit Parallel	E strobe(18-bit read data and 8-bit read parameter)

## 6.2 Serial Interface

The Module uses a 3-wire 9-bit serial interface or 4-pins/8bits bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: CSX (chip enable), SCL(serial clock) and SDA(serial data input/output) and the 4-pins serial use: CSX(chip enable), D/XC(data/ command select), SCL(serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

**Table 6.2.1 Serial Interface Type Selection**

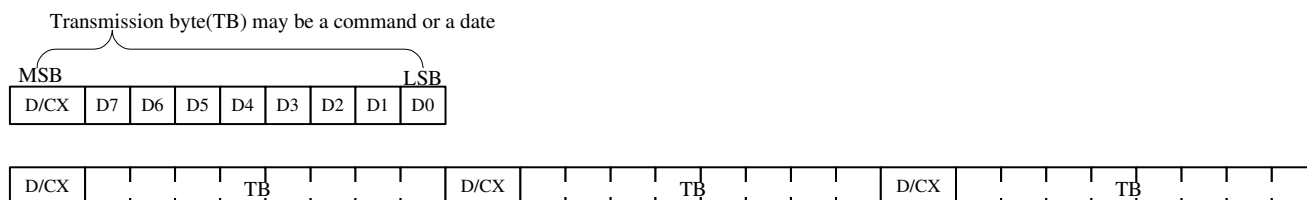
IM2	4WSPI	Interface	Read back selection
0	0	3-Pins Serial Interface	Via the read instruction(8-bits, 24-bits and 32-bits read parameter)
0	1	4-Pins Serial Interface	Via the read instruction(8-bits, 24-bits and 32-bits read parameter)

### 6.2.1 Command Write

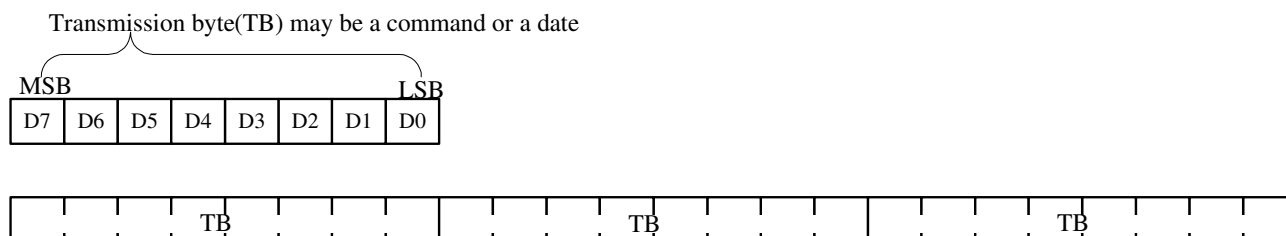
The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-Pins serial data packet contains a control bit D/CX and a transmission byte and in 4-pins serial case, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the Driver. The MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicated the start of data transmission.

**Figure1: 3-pins Serial Data Stream Format**

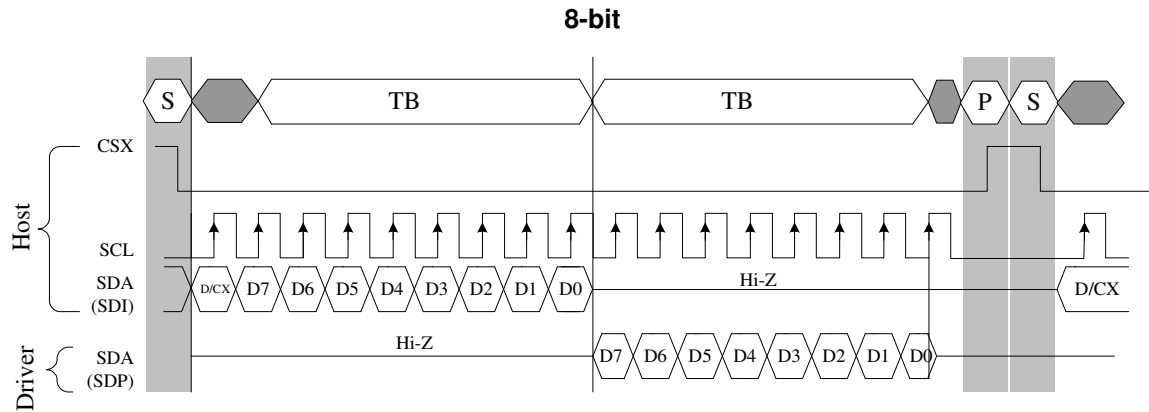


**Figure2: 4-pins Serial Data Stream Format**

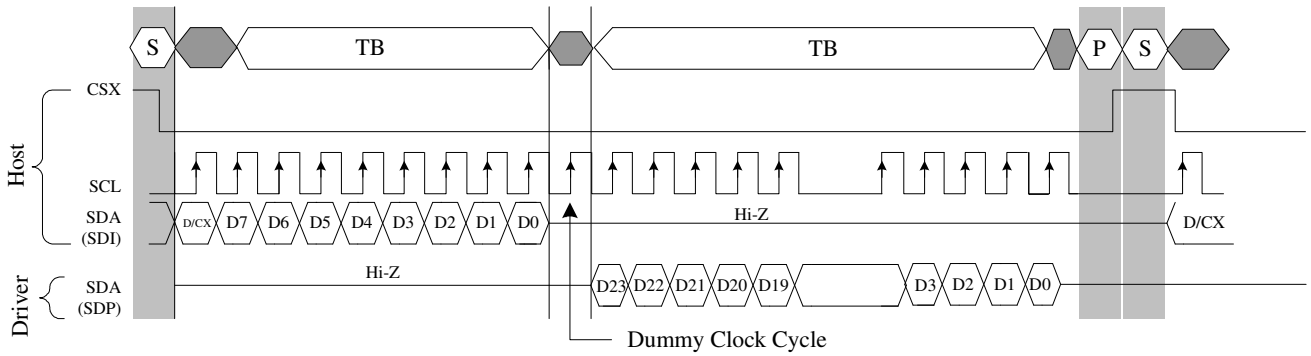


When CSX is “high”, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX=’0’) or parameter/RAM data (D/CX=’1’). It is sampled when first rising edge of SCL (3-pin serial interface) or 8<sup>th</sup> rising edge of SCL (4-pins serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-pin serial interface) or D7(4-pins serial interface) of the next byte at the next rising edge of SCL.

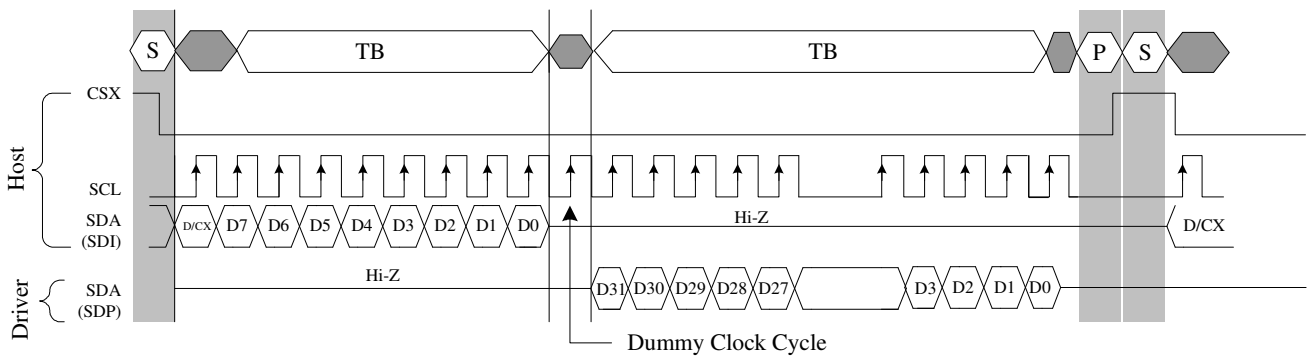
## 6.2.2 Read Function



**Figure3: 3-Pin Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:**



**Figure4: 3-Pin Serial Protocol (for RDDID command: 24-bit read)**



**Figure5: 3-Pin Serial Protocol (for RDDST command: 32-bit read)**

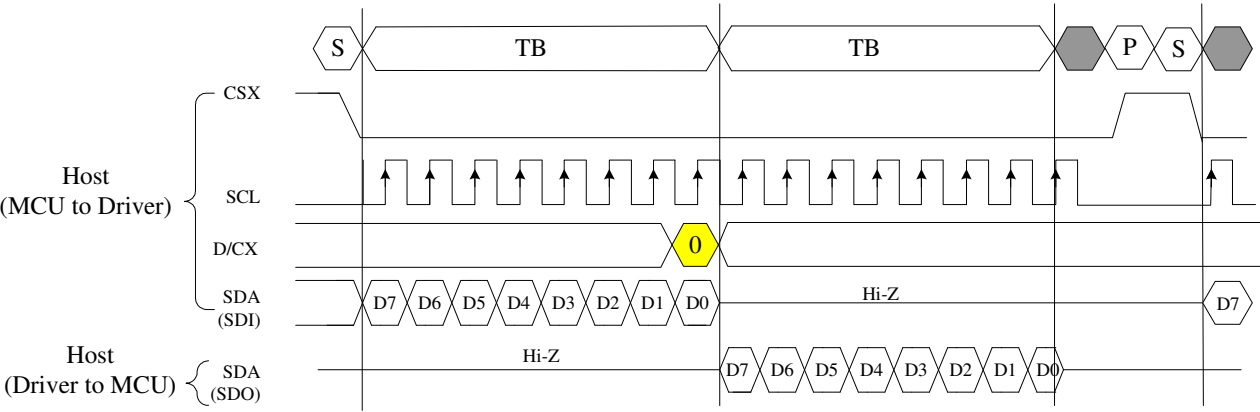


Figure6:Tm [(C)

### 6.3 8080-Series Parallel Interface (P68='0')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The graphics controller chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17,0] bits are display RAM data or command parameters. When D/C='0', D[17,0] bits are commands.

The 8080-series bi-direction interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (GND). Interface bus width can be selected with IM2, IM1 and IM0. The interface function of 8080-series parallel interface are given in Table 6.3.1.

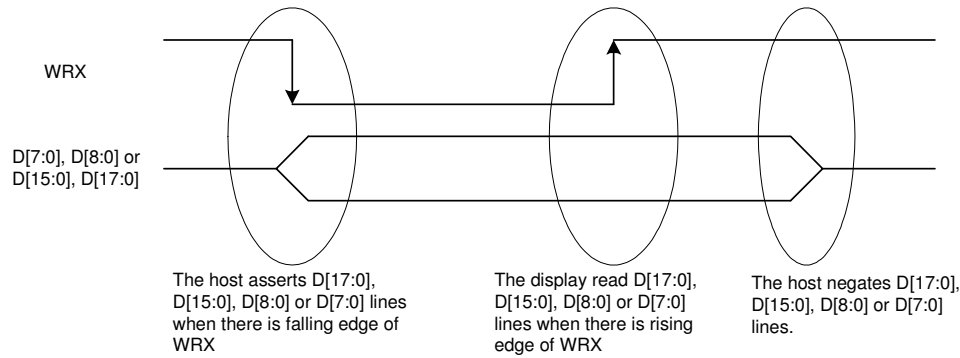
**Table 6.3.1 The function of 8080-series parallel interface**

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	1	0	0	8-bit Parallel	0	1	↑	Write 8-bit command(D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter(D7 to D0)
					1	↑	1	Read 8-bit display data(D7 to D0)
					1	↑	1	Read 8-bit parameter or status(D7 to D0)
0	1	0	1	16-bit Parallel	0	1	↑	Write 8-bit command(D7 to D0)
					1	1	↑	Write 16-bit display data or 8-bit parameter(D15 to D0)
					1	↑	1	Read 16-bit display data(D15 to D0)
					1	↑	1	Read 8-bit parameter or status(D7 to D0)
0	1	1	0	9-bit Parallel	0	1	↑	Write 8-bit command(D7 to D0)
					1	1	↑	Write 9-bit display data or 8-bit parameter(D8 to D0)
					1	↑	1	Read 9-bit display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status(D7 to D0)
0	1	1	1	18-bit Parallel	0	1	↑	Write 8-bit command(D7 to D0)
					1	1	↑	Write 18-bit display data or 8-bit parameter(D17 to D0)
					1	↑	1	Read 18-bit display data(D17 to D0)
					1	↑	1	Read 8-bit parameter or status(D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

#### 6.3.1 Write Cycle/Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17...0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (= '0') and vice versa it is data (= '1'). The write cycle is described in the following figure.



Note: WRX is an unsynchronized signal (it can be stopped)

Figure9: 8080-Series WRX Protocol

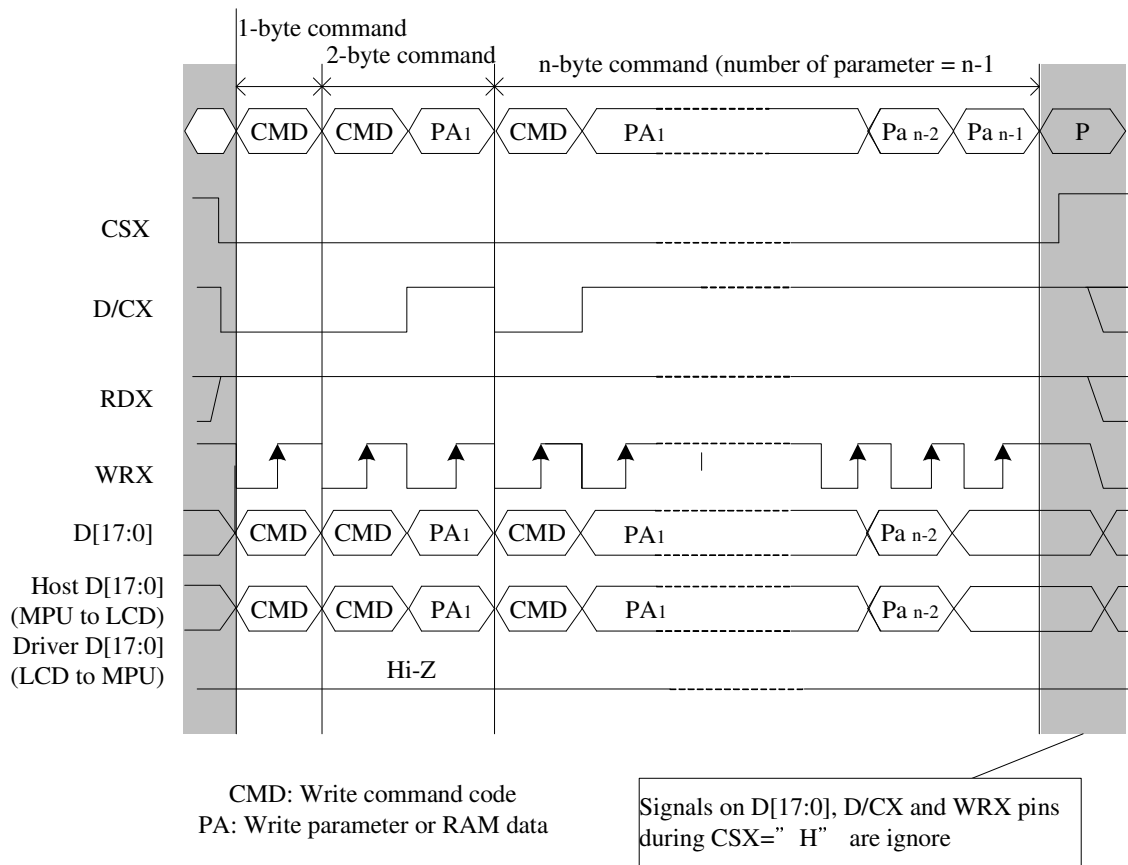
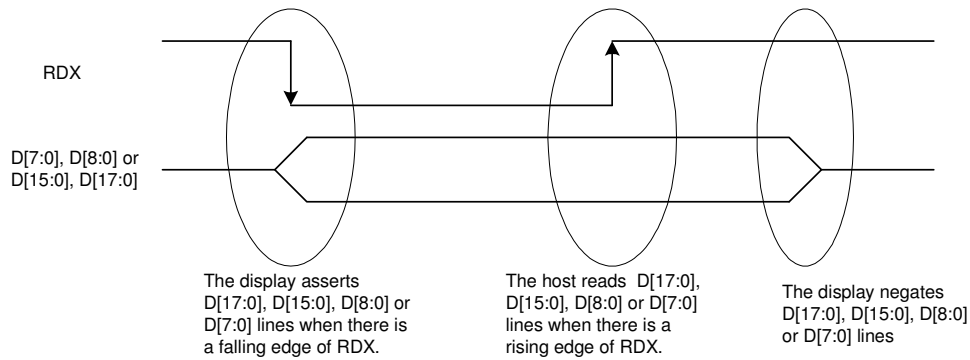


Figure10: 8080-Series Parallel bus protocol (write to register or display RAM)

### 6.3.2 Read Cycle/Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from the display via interface. The display sends data (D[17...0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure11: 8080-Series RDX Protocol

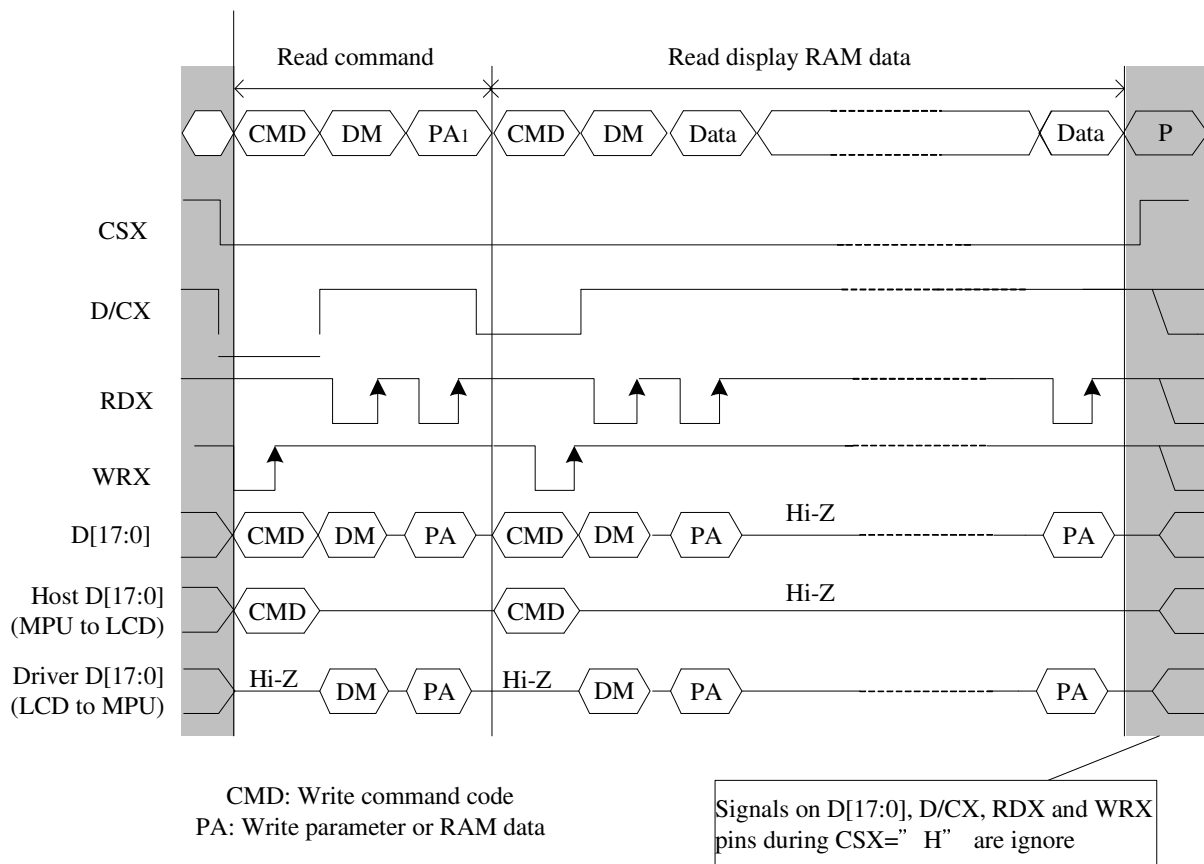


Figure12: 8080-Series parallel bus protocol (Read from register or display RAM)

## 6.4 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX(active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of E signal when R/WX='1' and writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17,0] bits are display RAM data or command parameters. When D/C='0', D[17,0] bits are commands.

The 6800-series bi-direction interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0. The interface function of 6800-series parallel interface are given in Table 6.4.1.

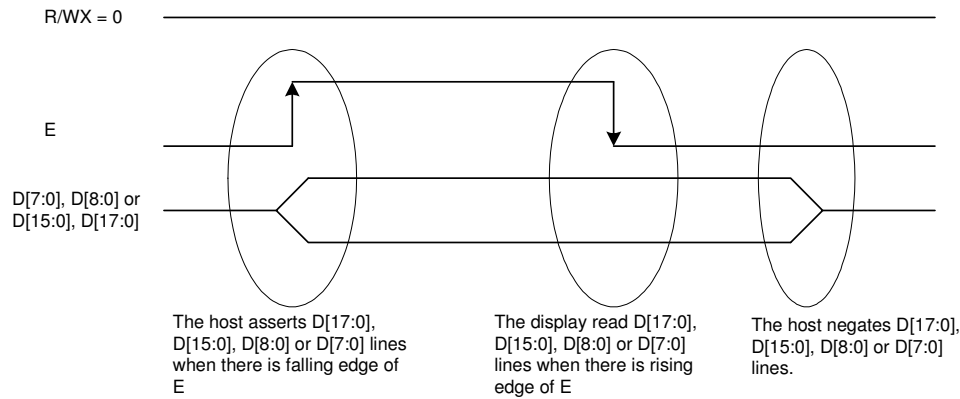
**Table 6.4.1 The function of 6800-series parallel interface**

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
1	1	0	0	8-bit Parallel	0	1	↓	Write 8-bit command(D7 to D0)
					1	1	↓	Write 8-bit display data or 8-bit parameter(D7 to D0)
					1	↓	1	Read 8-bit display data(D7 to D0)
					1	↓	1	Read 8-bit parameter or status(D7 to D0)
1	1	0	1	16-bit Parallel	0	1	↓	Write 8-bit command(D7 to D0)
					1	1	↓	Write 16-bit display data or 8-bit parameter(D15 to D0)
					1	↓	1	Read 16-bit display data(D15 to D0)
					1	↓	1	Read 8-bit parameter or status(D7 to D0)
1	1	1	0	9-bit Parallel	0	1	↓	Write 8-bit command(D7 to D0)
					1	1	↓	Write 9-bit display data or 8-bit parameter(D8 to D0)
					1	↓	1	Read 9-bit display data (D8 to D0)
					1	↓	1	Read 8-bit parameter or status(D7 to D0)
1	1	1	1	18-bit Parallel	0	1	↓	Write 8-bit command(D7 to D0)
					1	1	↓	Write 18-bit display data or 8-bit parameter(D17 to D0)
					1	↓	1	Read 18-bit display data(D17 to D0)
					1	↓	1	Read 8-bit parameter or status(D7 to D0)

Note : applied for command code : DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

### 6.4.1 Write Cycle/Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17...0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (= '0') and vice versa it is data (= '1'). The write cycle is described in the following figure.



Note: E is unsynchronized signal (it can be stopped)

Figure13: 6800-Series Write Protocol

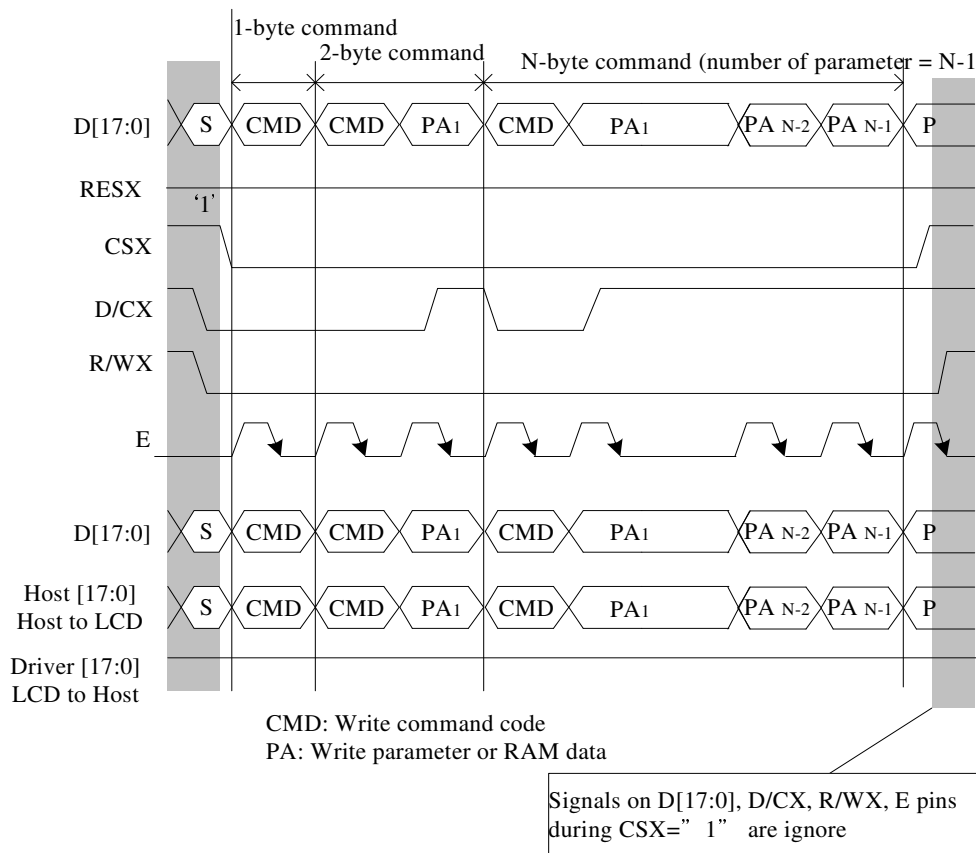
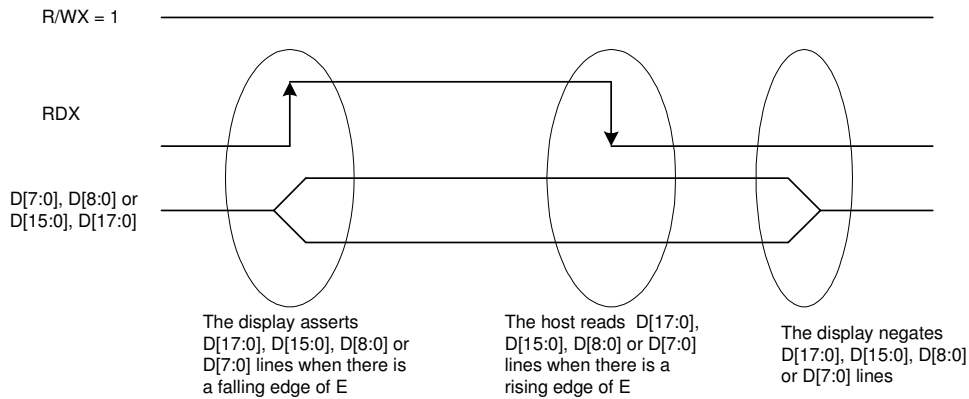


Figure14: 6800-Series parallel bus protocol (write to register or display RAM)

## 6.4.2 Read Cycle/Sequence

The read cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data (D[17...0]). D/CX bit is control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=‘0’) and vice versa it is data (=‘1’)



Note: E is an unsynchronized signal (It can be stopped).

Figure15: 6800-Series Read Protocol

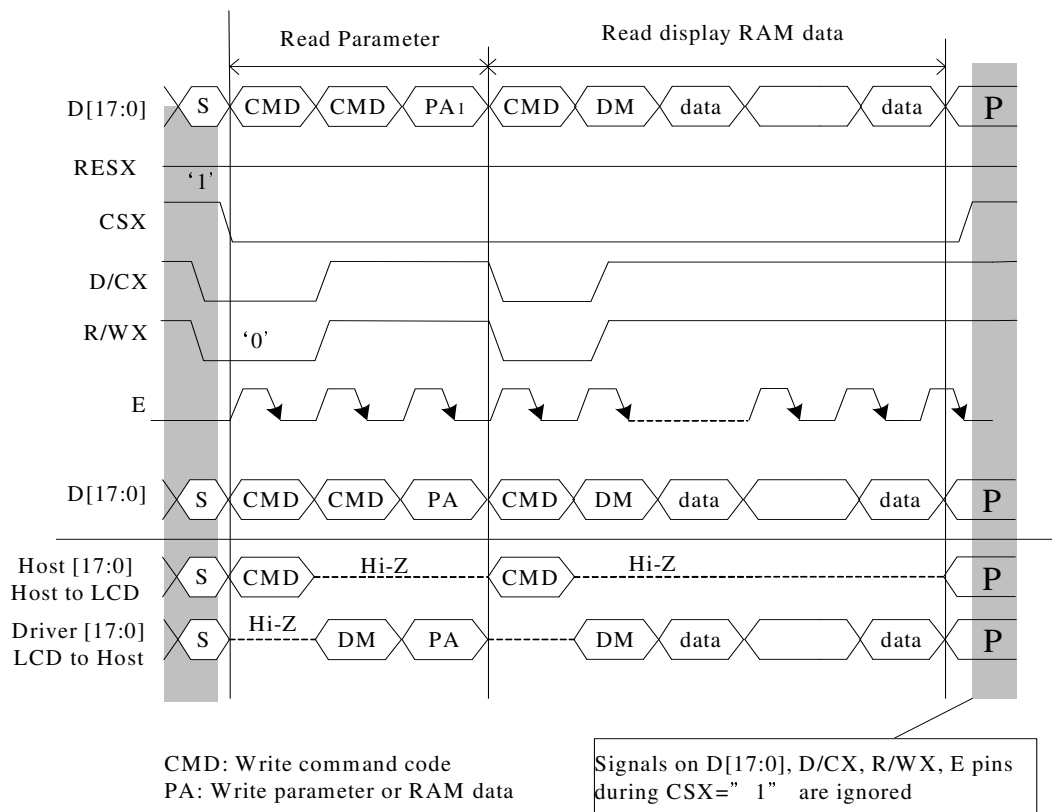


Figure16: 6800-Series Parallel bus protocol (Read from register or display RAM)

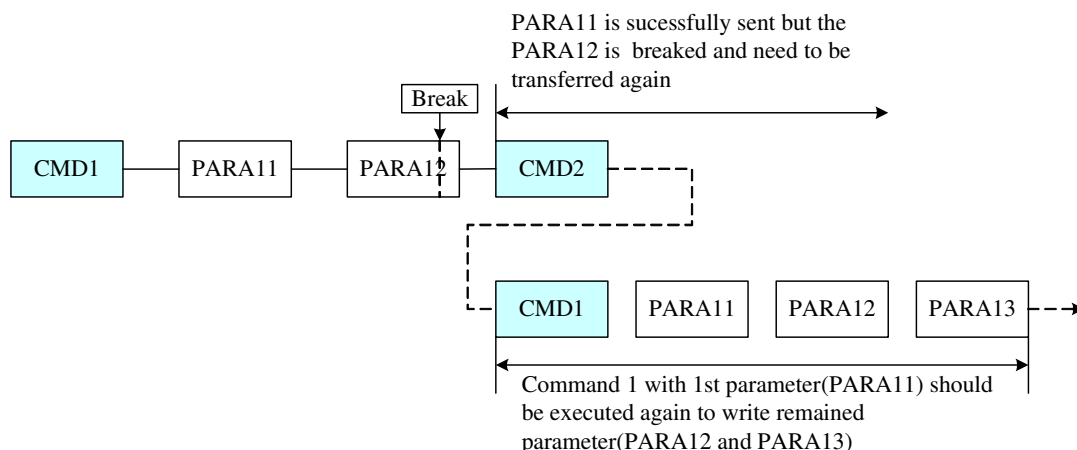
## 6.5 Display Data Transfer Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous its and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example.



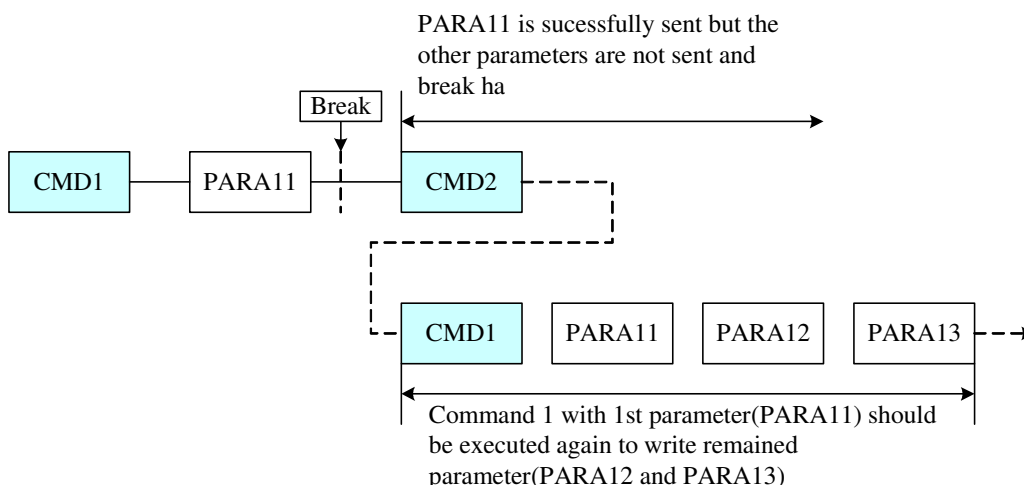
## 6.6 Display Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below:



**Figure19: Write interrupts recovery (serial interface)**

If 1, 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of command remains previous value.



**Figure20: Write interrupts recovery (both serial and parallel interface)**

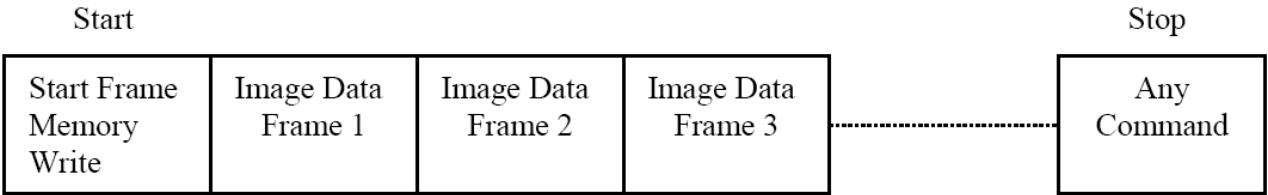


## 6.7 Display Data Transfer Mode

The Module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

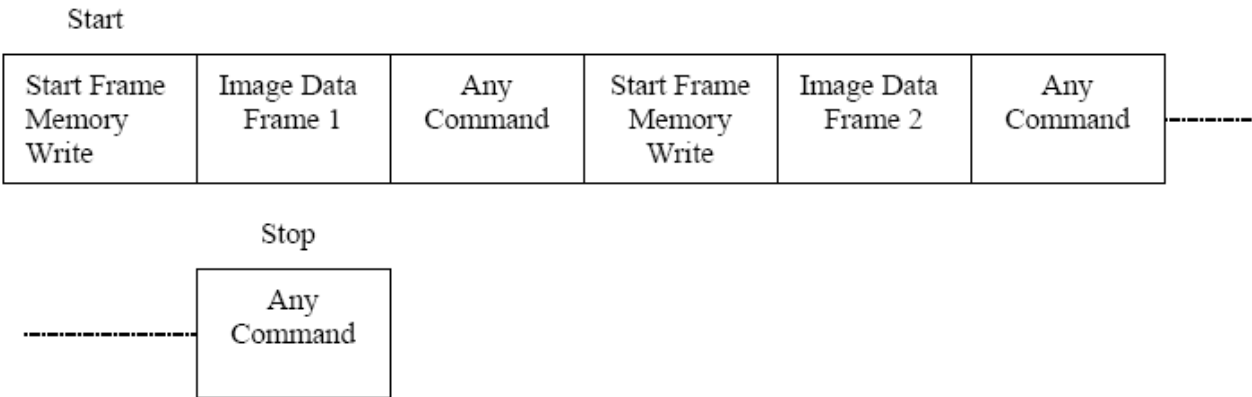
### Method 1:

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



### Method 2:

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

1. These apply to this Data Transfer Color mode on both Serial and Parallel interfaces.
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

## 6.8 RGB Interface

### 6.8.1 RGB Interface Selection

The RGB interface mode is available for ILI9163C and the interface is selected by setting the VIPF[3:0] bits as following table.

VIPF[3:0]				RGB Interface	Data Bus
0	1	1	0	18-bit RGB interface	D[17:0]
0	1	0	1	16-bit RGB interface	D[17:13], D[11:1]
1	1	1	0	6-bit RGB interface	D[7:2]
Others				Setting prohibited	

The display operation via RGB interface is synchronized with the VS, HS and PCLK signals. The RGB interface transfers the updated data to GRAM and the update area is defined by the window address function. The back porch and back porch are used to set the RGB interface timing.

### Parallel RGB Interface Set Table

18-bit data bus interface (D[17:0] is used) , VIPF[3:0] = 0110

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] and D[11:1] are used) , VIPF[3:0] = 0101

	D17	D16	D15	D14	D13	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (D[7:2] is used) , VIPF[3] = 1110

	First Transfer						Second Transfer						Third Transfer					
	D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, EN and D[17:0] states when there is a rising edge of the PCLK. The PCLK can not be used as continues internal clock for other functions of the display module.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is high enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (EN) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal. D[17:0] are used to tell what is the information of the image that is transferred on the display (When EN= '1' and there is a rising edge of PCLK). D[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.

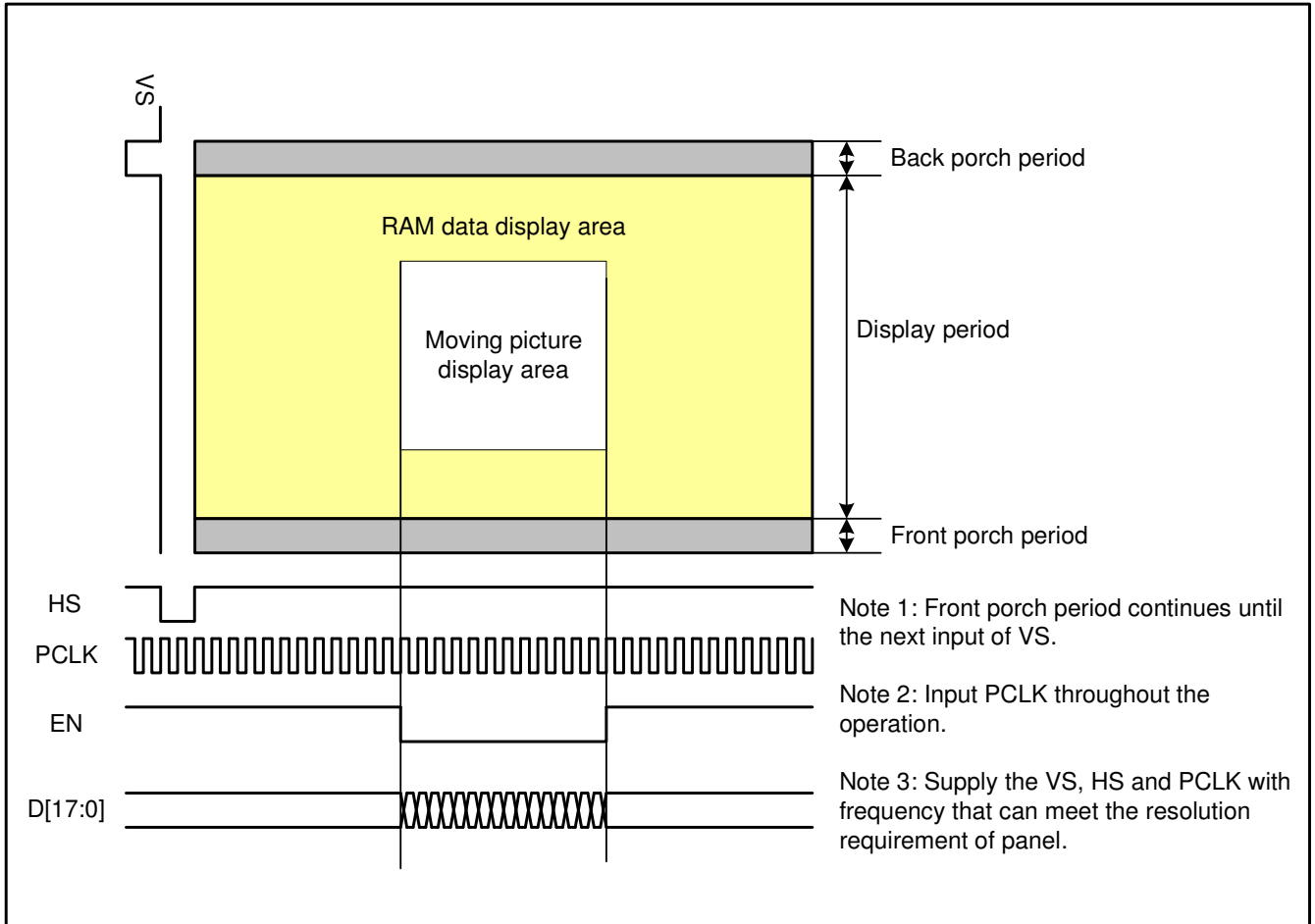


Figure23: GRAM Access Area by RGB Interface

## 6.8.2 RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

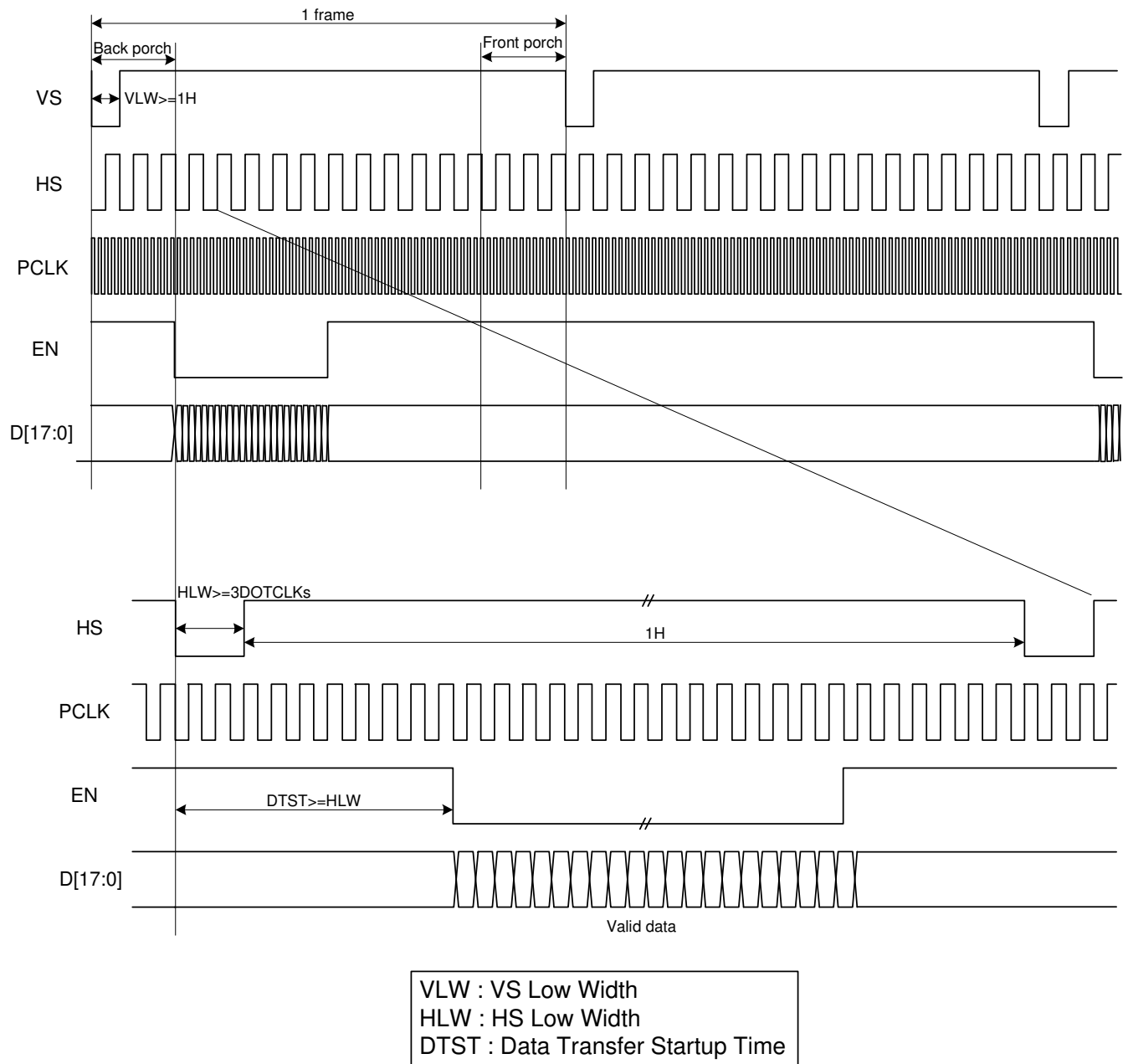
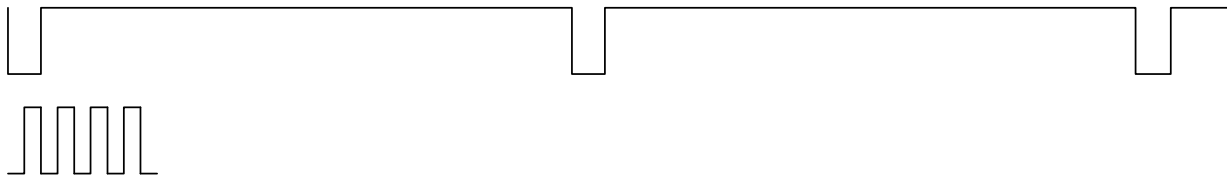


Figure24: Timing Chart of Signals in 18-/16-bit RGB Interface Mode



The timing chart of 6-bit RGB interface mode is shown as below:



### 6.8.3 RGB Interface Mode Set

ILI9163C supplies a RGB interface with DE mode and can be controlled by external RCM[1:0] pins.

RCM1	RCM0	Resolution selection
0	0	MCU interface mode
0	1	MCU interface mode
1	0	RGB interface(1)
1	1	RGB interface(2)

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

**In RGB Mode 1 :** (RCM1, RCM0 = “10”), writing data to frame memory is done by PCLK and Video Data Bus , when DE is high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to driver.

**In RGB Mode 2 :** (RCM1, RCM0 = “11”), blanking porch setting of VS and HS signals are defined by RGBBPCTR (B5h)command. DE pin is used for data making. When DE pin is high, valid data is directly stored to frame memory. In the contrast, if DE pin is low, valid data will becomes “00” and stored to frame memory.

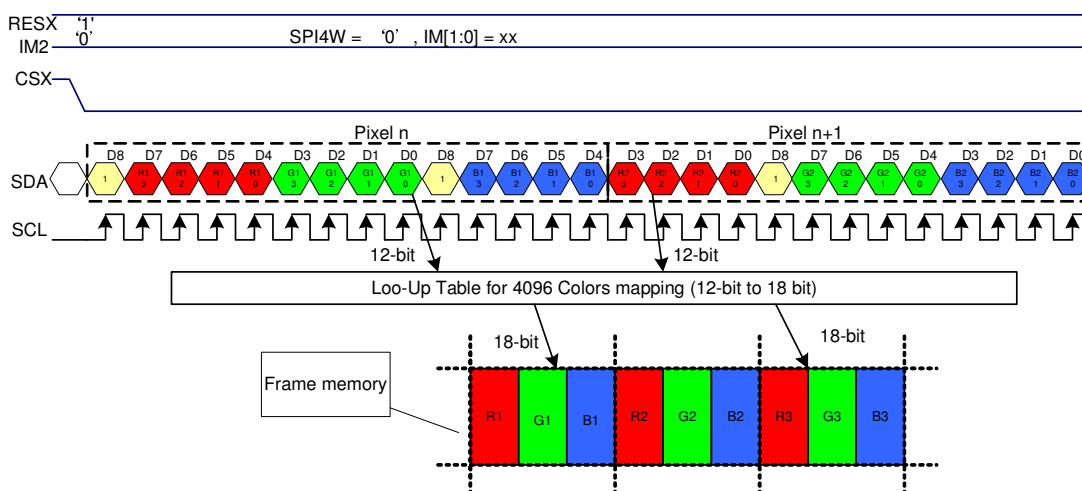
## 6.9 Display Data Color Coding

### 6.9.1 Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.

- ✧ 4k colors, RGB 4-4-4-bits input
- ✧ 65K colors, RGB 5-6-5-bits input
- ✧ 262K colors, RGB 6-6-6-bits input

3-pin 9-bit data protocol



Note 1: pixel data with the 12-bits color depth information.

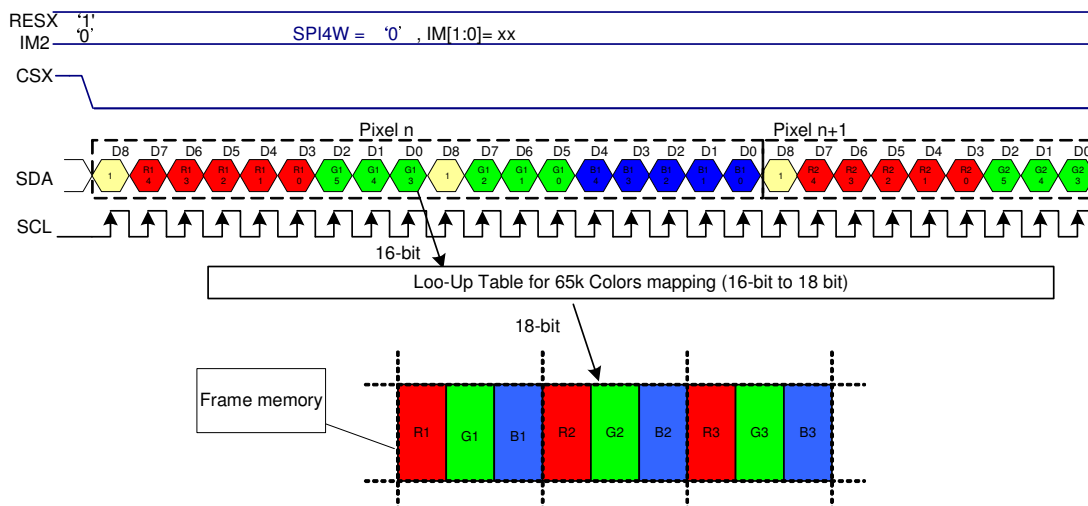
Note 2: The most significant bits are:  $Rx^3$ ,  $Gx^3$  and  $Bx^3$

Note 3: The least significant bits are:  $Rx^0$ ,  $Gx^0$  and  $Bx^0$

Note 4: X = don't care – Can be set to '0' or '1'

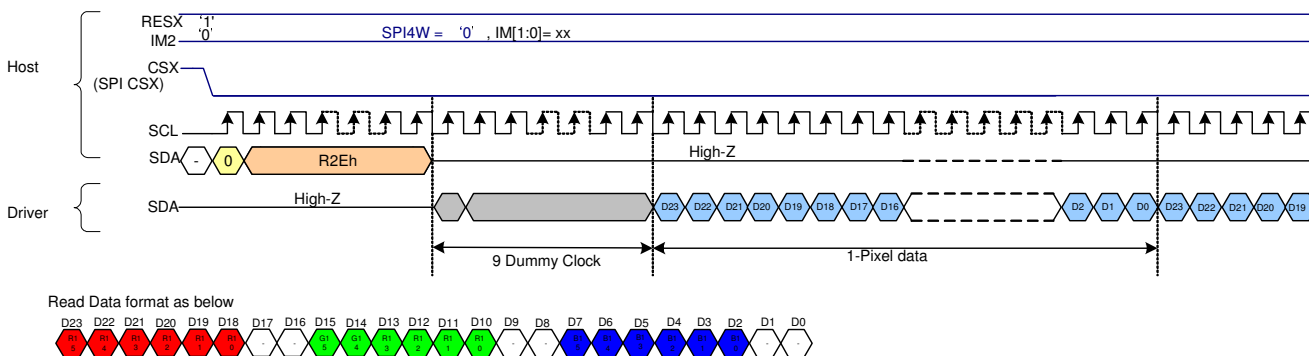
**Figure26: Write data for RGB4-4-4 bits input**

4-pin 8-bit Series data protocol



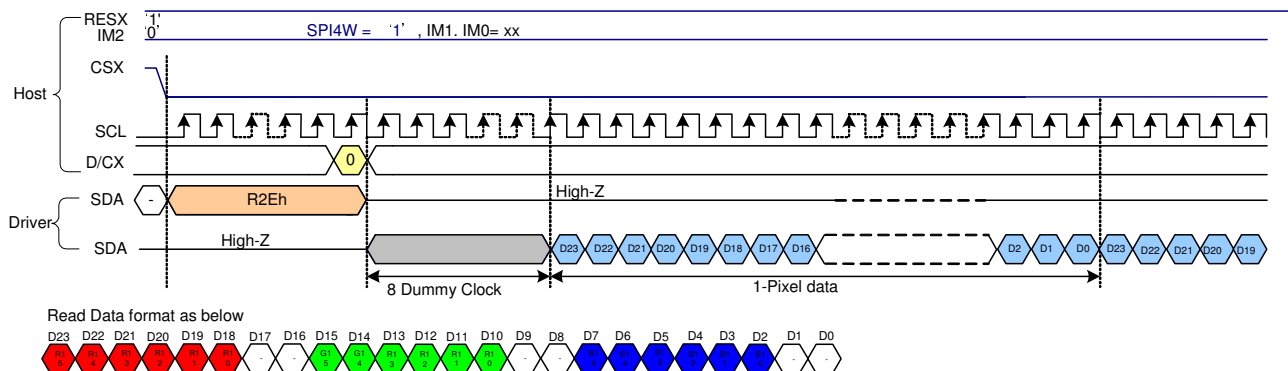
Note 4: X = Don't care – Can be set to '0' or '1'

### Read data for 3-W SPI RGB



Note: X = Don't care – Can be set to '0' or '1'

### Read data for 4-W SPI RGB



Note: X = Don't care – Can be set to '0' or '1'

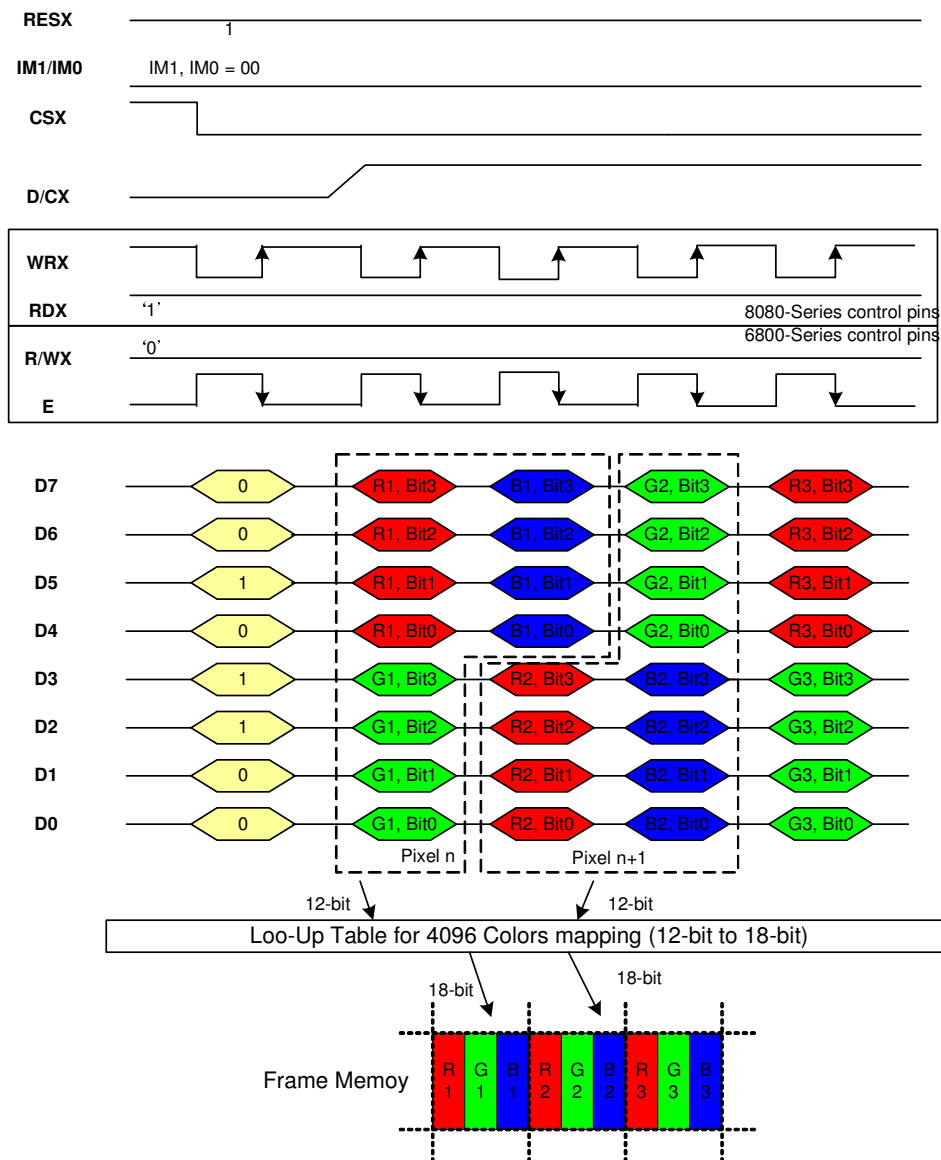
Figure29: Read data for SPI RGB 6-6-6-bits

## 6.9.2 8-bit Parallel Interface (IM2='1', IM[1:0] = "00")

Different display data formats are available for three colors depth supported by listed below

- ✧ 4k colors, RGB4-4-4-bits input
- ✧ 65K colors, RGB5-6-5-bits input
- ✧ 262K colors, RGB6-6-6-bits input

2 pixels (6 sub-pixels) per 3 transfer



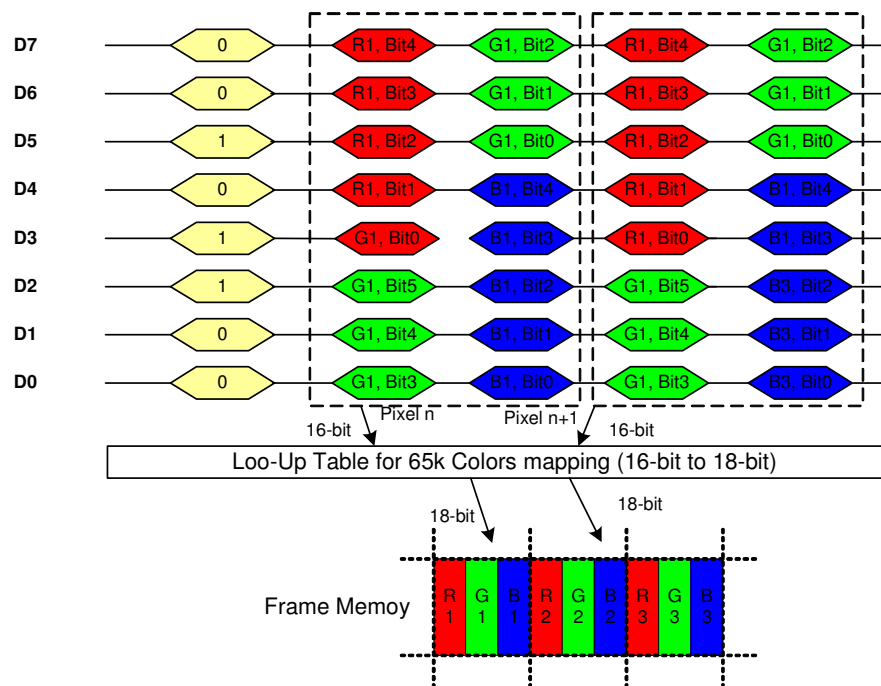
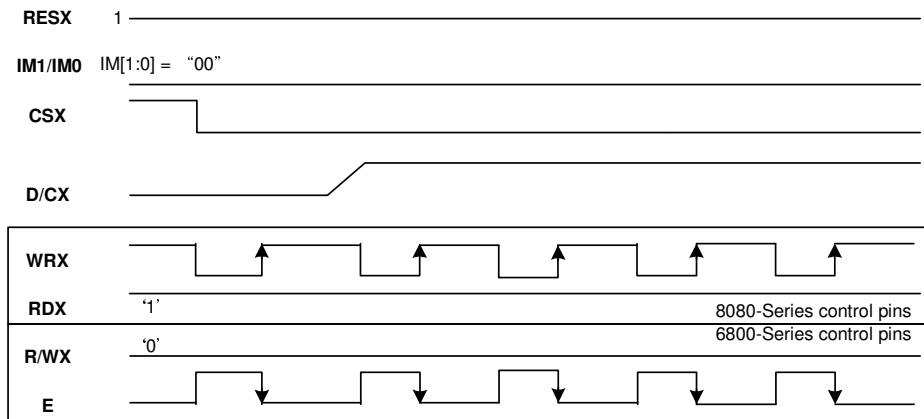
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

Figure30: Write 8-bit data for RGB 4-4-4-bits input

1 pixel (3 sub-pixels) per 2 transfer



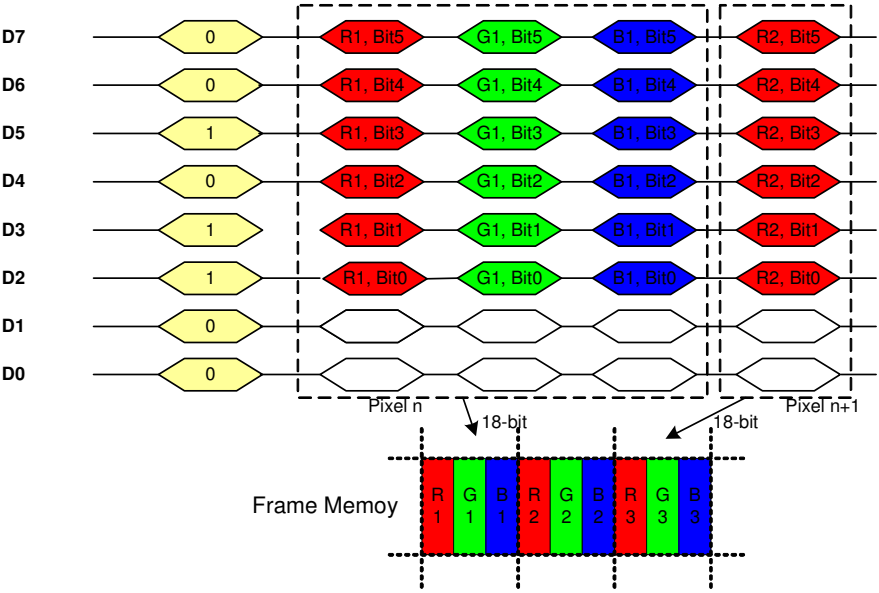
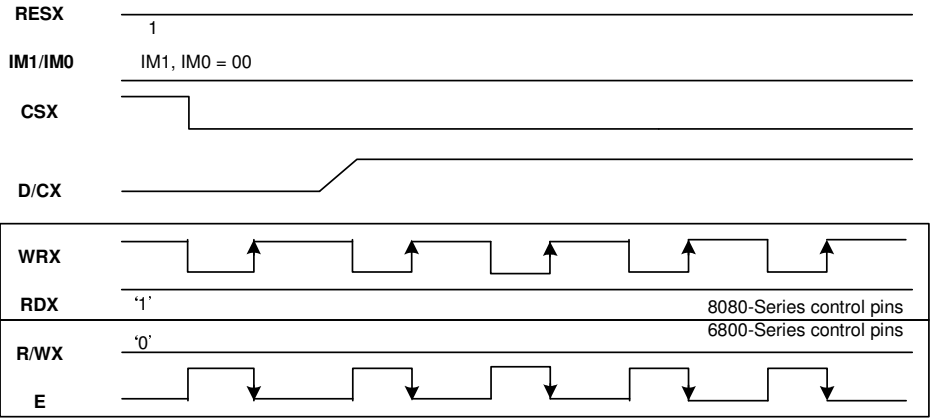
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit3, LSB=Bit 0 for Green and MSB=Bit4, LSB=Bit0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

Figure31: Write 8-bits data for RGB 5-6-5-bits input

1 pixel (3 sub-pixels) per 3 transfer



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit5, LSB=Bit 0 for Red, Green and Blue data.  
 Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.  
 Note 3: '-' = Don't care – Can be set to '0' or '1'

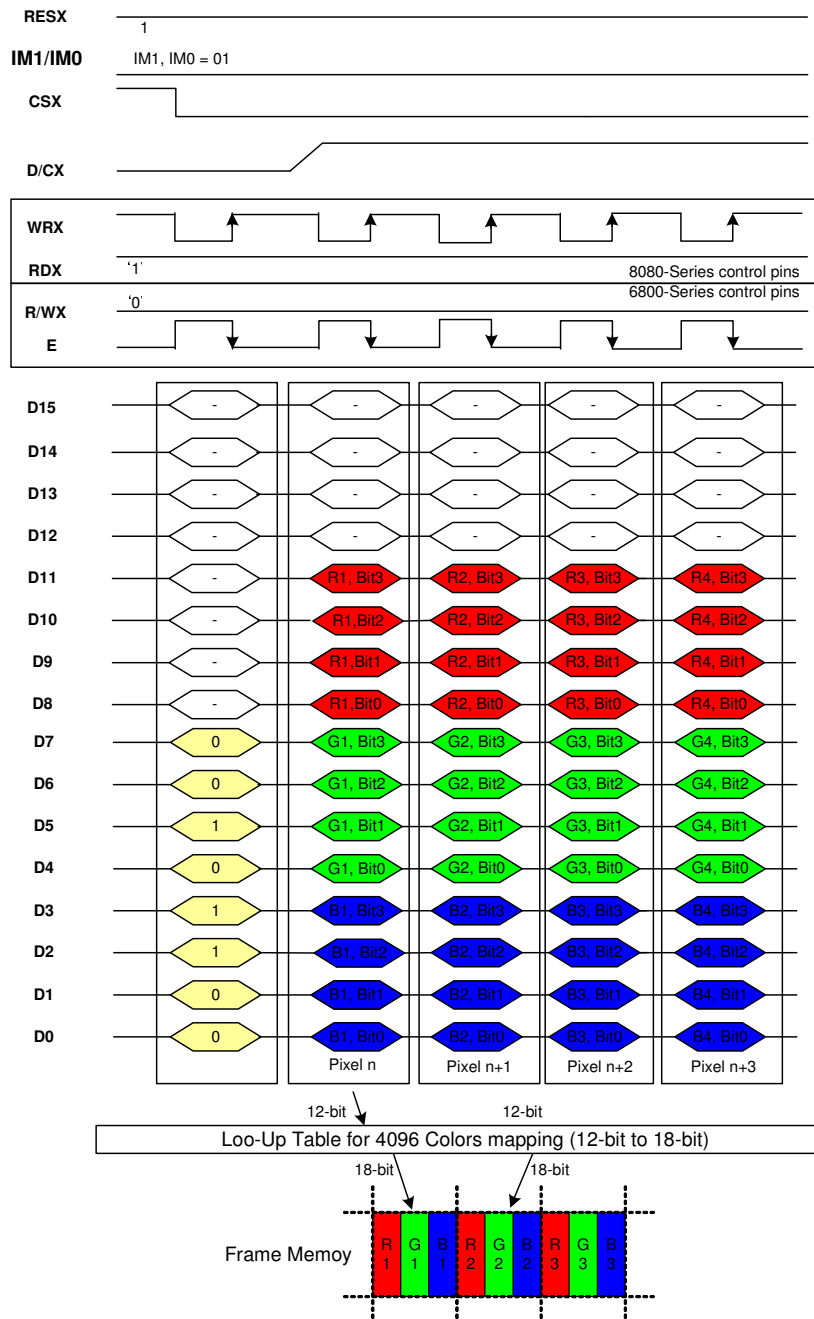
Figure32: Write 8-bit data for RGB 6-6-6-bits input

### 6.9.3 16-bit Parallel Interface (IM2='1', IM1, IM0='01')

Different display data formats are available for three colors depth supported by listed below

- ✧ 4k colors, RGB 4-4-4-bits input
- ✧ 65K colors, RGB 5-6-5-bits input
- ✧ 262K colors, RGB 6-6-6-bits input

1 pixels (3 sub-pixels) per 1 transfer, 12-bits/pixel



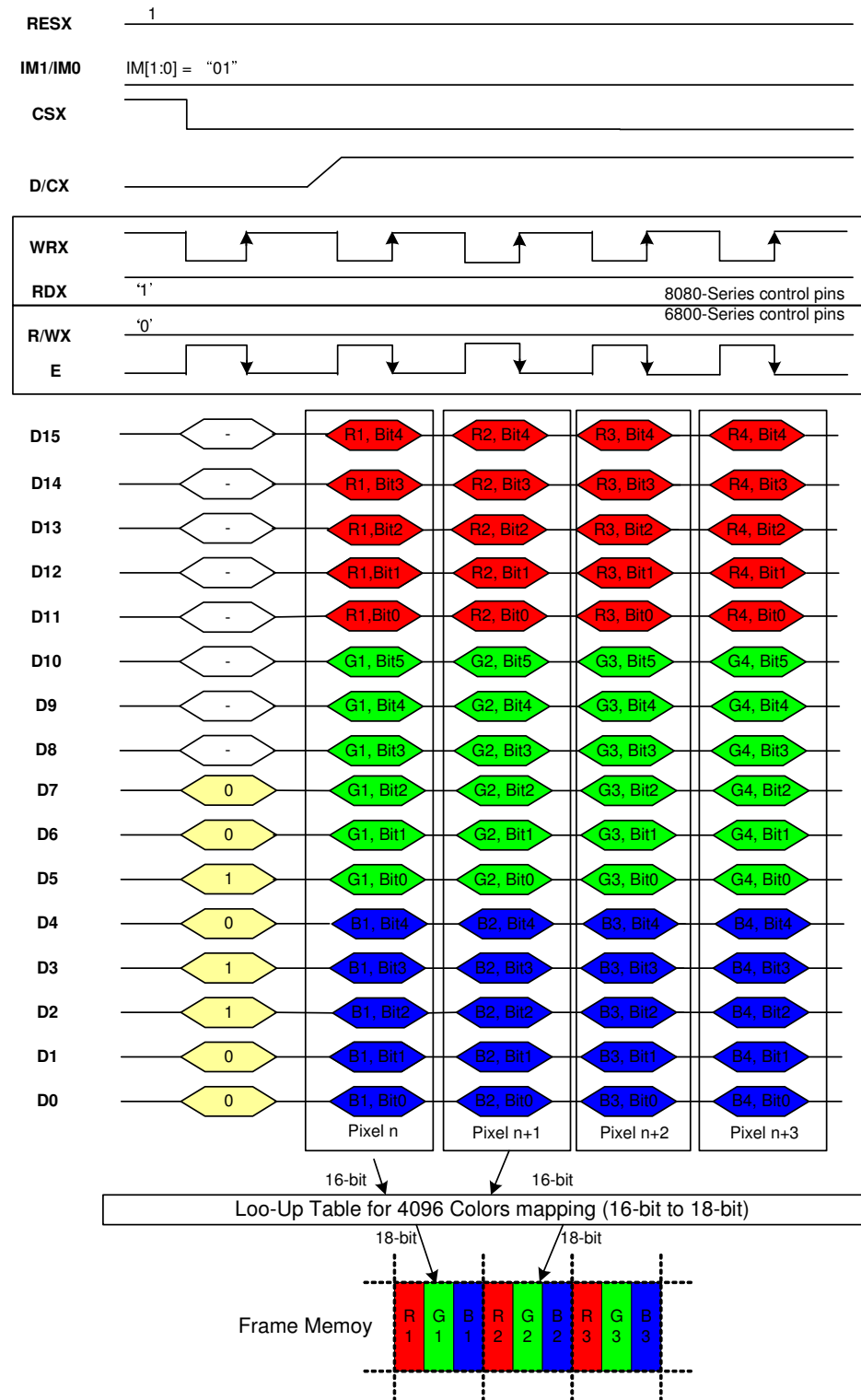
Note1: The data order is as follows, MSB = D15, LSB = D0 and picture data is MSB = Bit3, LSB = Bit0 for Red, Green and Blue data.

Note 2: 1-times transfer (D7 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3: '=' Don't care – Can be set to '0' or '1'

Figure33: Write 16-bit data for RGB4-4-4-bits input (4k-color)

1 pixel (3 sub-pixels) per 1 transfer, 16-bits/pixel



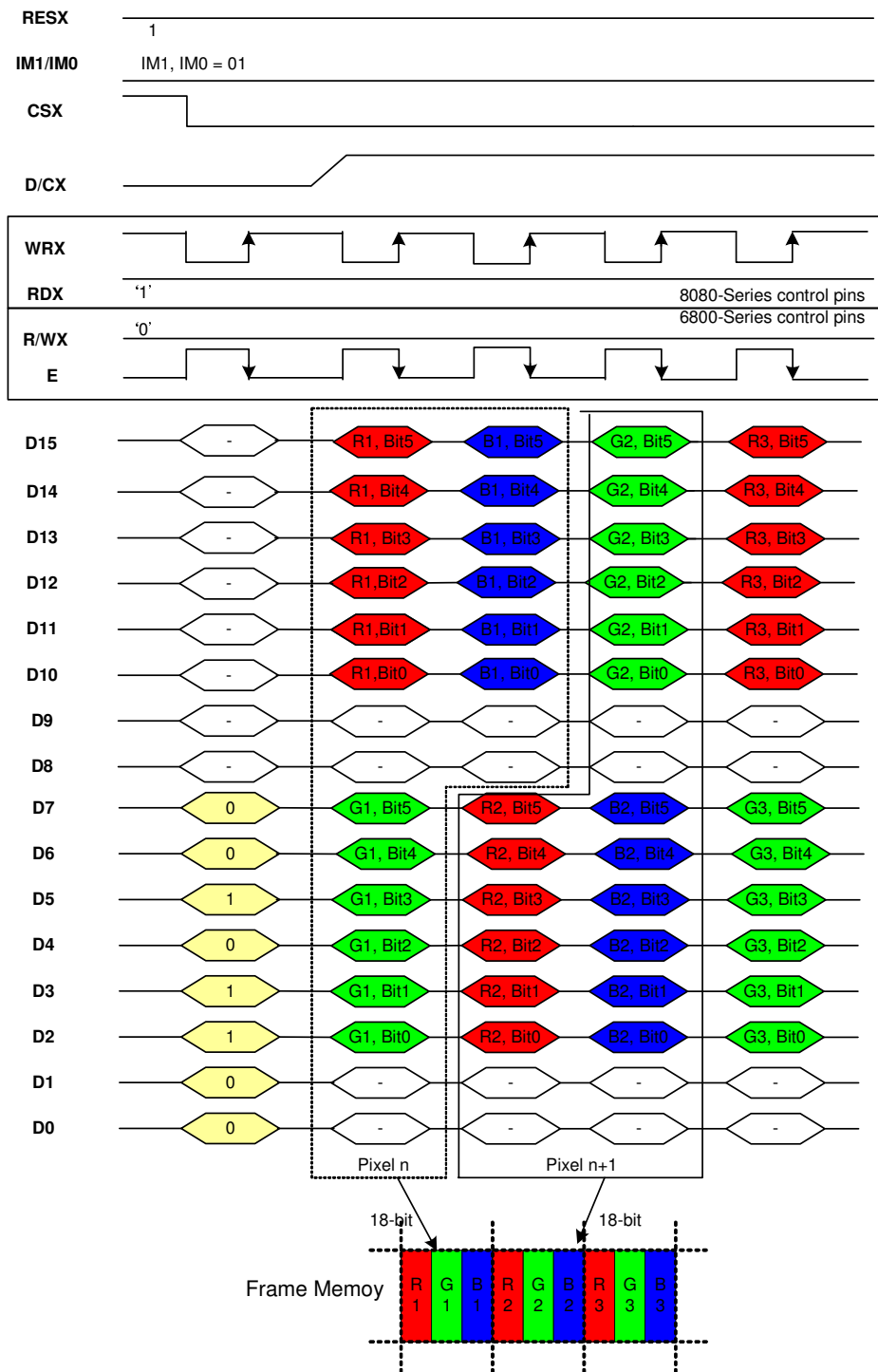
Note1: The data order is as follows, MSB = D15, LSB = D0 and picture data is MSB = Bit5, LSB = Bit0 for Red and Blue and MSB=Bit5, LSB=Bit 0 for Green data.

Note 2: 1-time transfer (D7 to D0) is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '=' Don't care – Can be set to '0' or '1'

Figure34: Write 16-bit data for RGB 5-6-5-bits input (65k colors)

2 pixels (6 sub-pixels) per 2 transfer, 18-bits/pixel



Note1: The data order is as follows, MSB = D15, LSB = D0 and picture data is MSB = Bit2, LSB = Bit0 for Red and Green and MSB=Bit1, LSB=Bit 0 for Blue data.

Note 2: 1-time transfer (D7 to D0) is used to transmit 1 pixel data with the 8-bit color depth information.

Note 3: '=' Don't care – Can be set to '0' or '1'

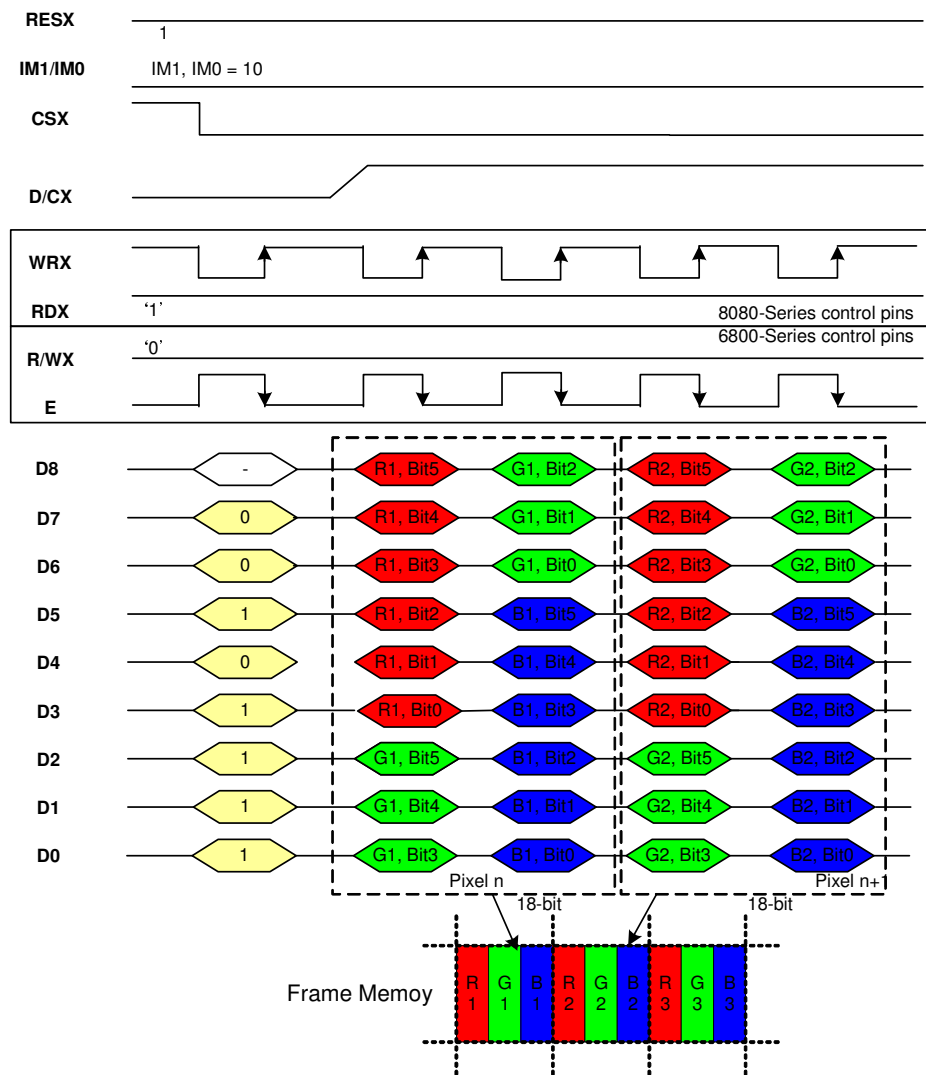
**Figure35: Write 16-bit data for RGB 6-6-6-bits input (262K colors)**

## 6.9.4 9-bit Parallel Interface (IM2='2', IM1, IM0="10")

Different display data formats are available for three colors depth supported by listed below

✧ 262K colors, RGB6-6-6-bits input

2 pixels (6 sub-pixels) per 4 transfer, 18-bits/pixel



Note1: The data order is as follows, MSB = D8, LSB = D0 and picture data is MSB = Bit5, LSB = Bit0 for Red and Green and Blue data.

Note 2: 3-times is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '=' Don't care – Can be set to '0' or '1'

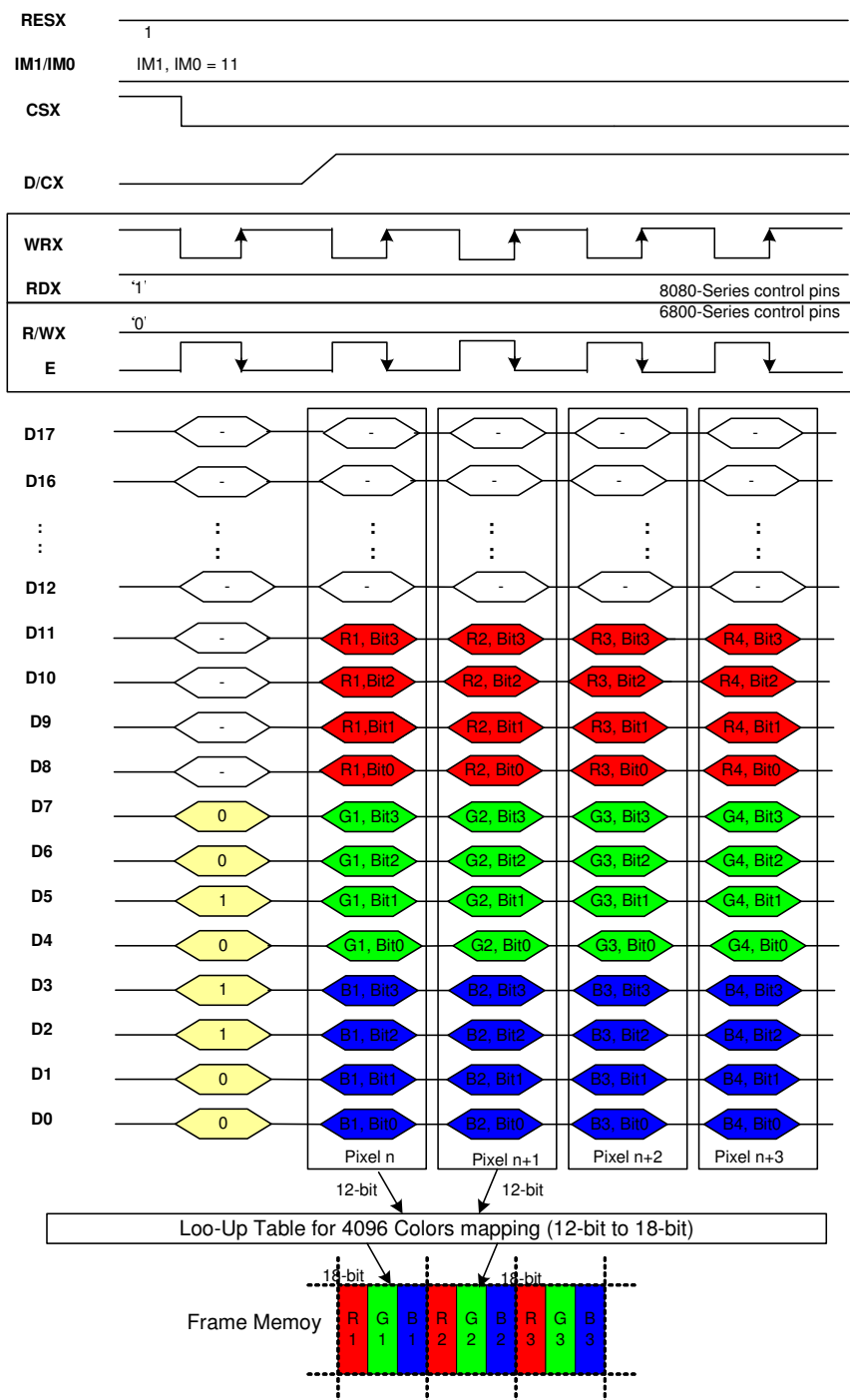
**Figure36: Write 9-bit data for RGB 6-6-6-bits input(262k-color)**

### 6.9.5 18-bit Parallel Interface (IM2='1', IM1, IM0="11")

Different display data formats are available for three colors depth supported by listed below

- ✧ 4k colors, RGB 4-4-4-bits input
- ✧ 65K colors, RGB 5-6-5-bits input
- ✧ 262K colors, RGB 6-6-6-bits input

1 pixel (3 sub-pixels) per 1 transfer, 12-bits/pixel

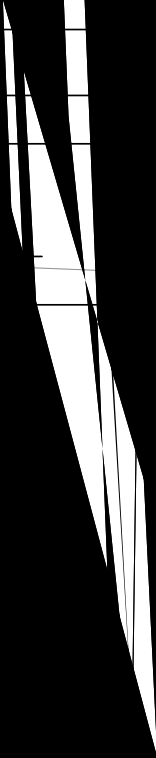


Note1: The data order is as follows, MSB = D11, LSB = D0 and picture data is MSB = Bit3, LSB = Bit0 for Red, Green and Blue data.

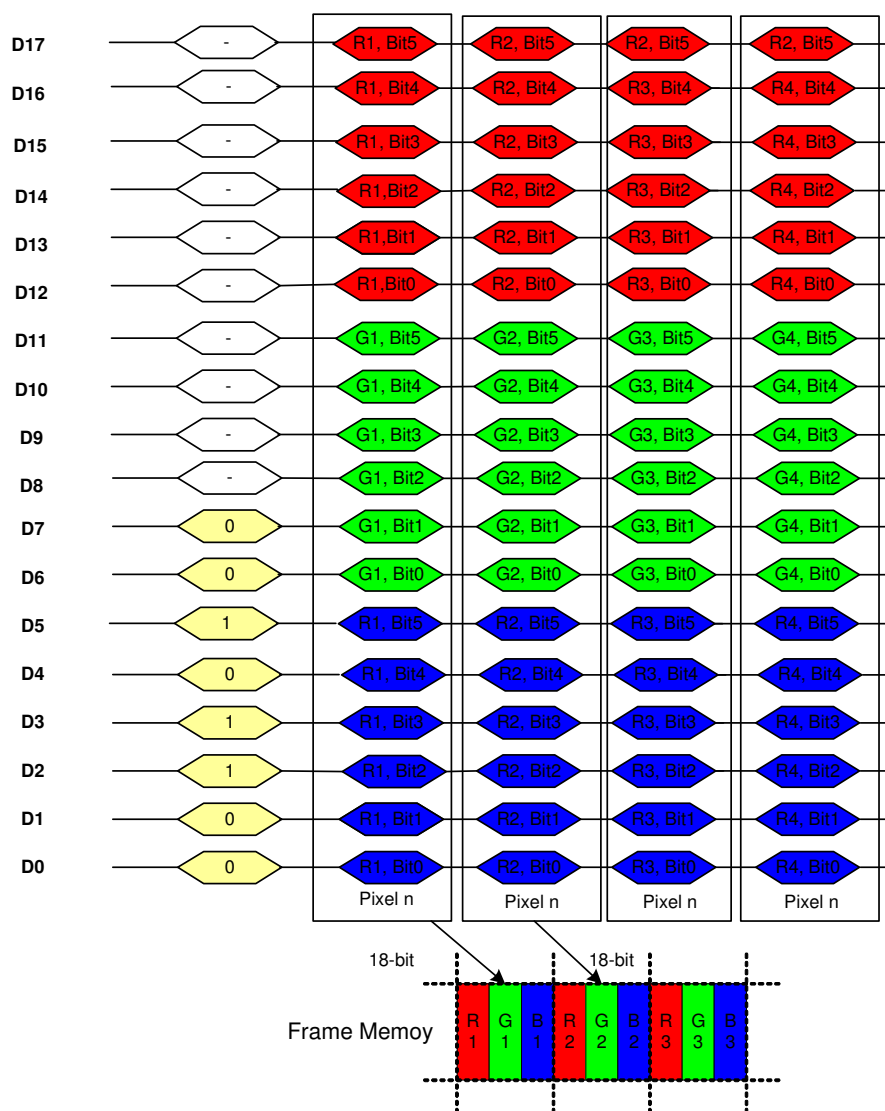
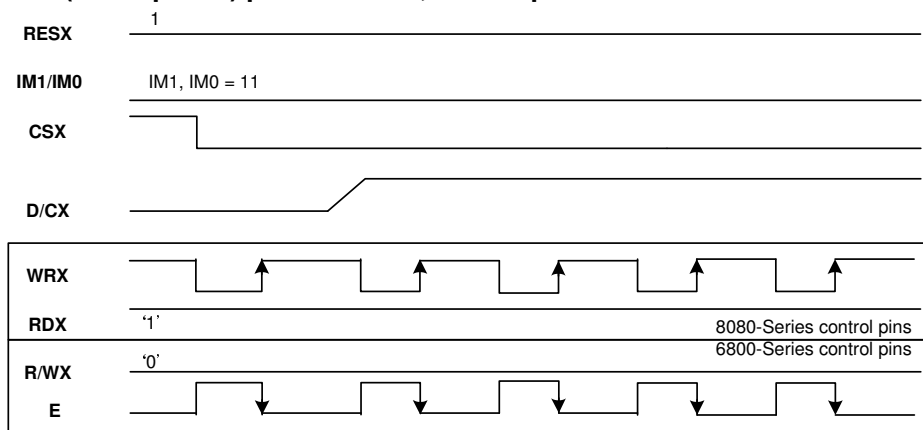
Note 2: 1-time is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3: '=' Don't care – Can be set to '0' or '1'

Figure37: Write 18-bits data for RGB 4-4-4-bits input (4k colors)



1 pixel (3 sub-pixels) per 1 transfer, 18-bits/pixel



Note1: The data order is as follows, MSB = D17, LSB = D0 and picture data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

Note 2: 1-time(D17 to D0) is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '=' Don't care – Can be set to '0' or '1'

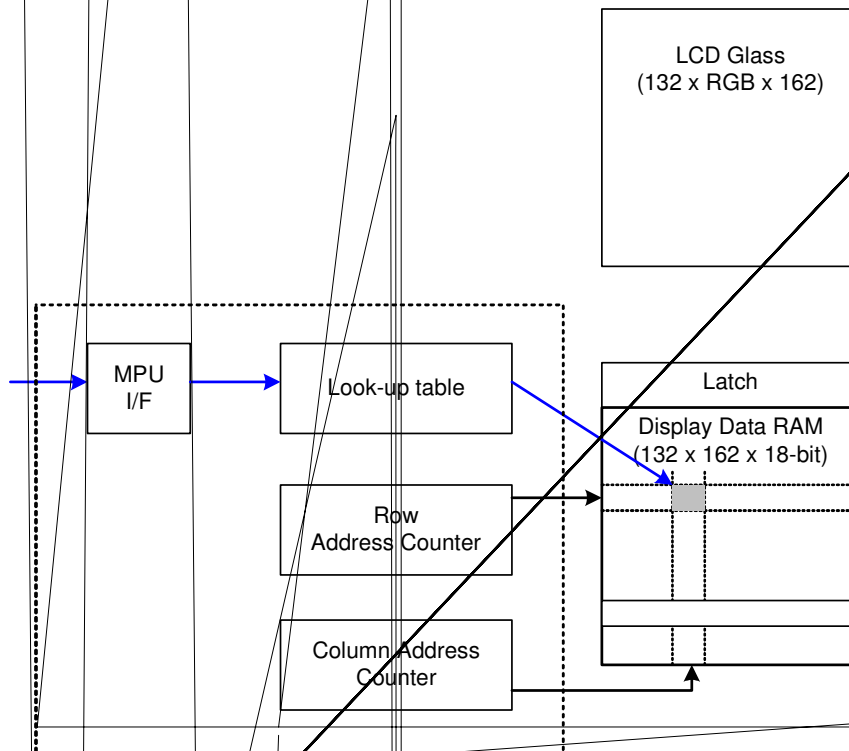
Figure39: Write 18-bit data for RGB 6-6-6-bits input (262K colors)

## 7. Display Data RAM

### 7.1 Configuration

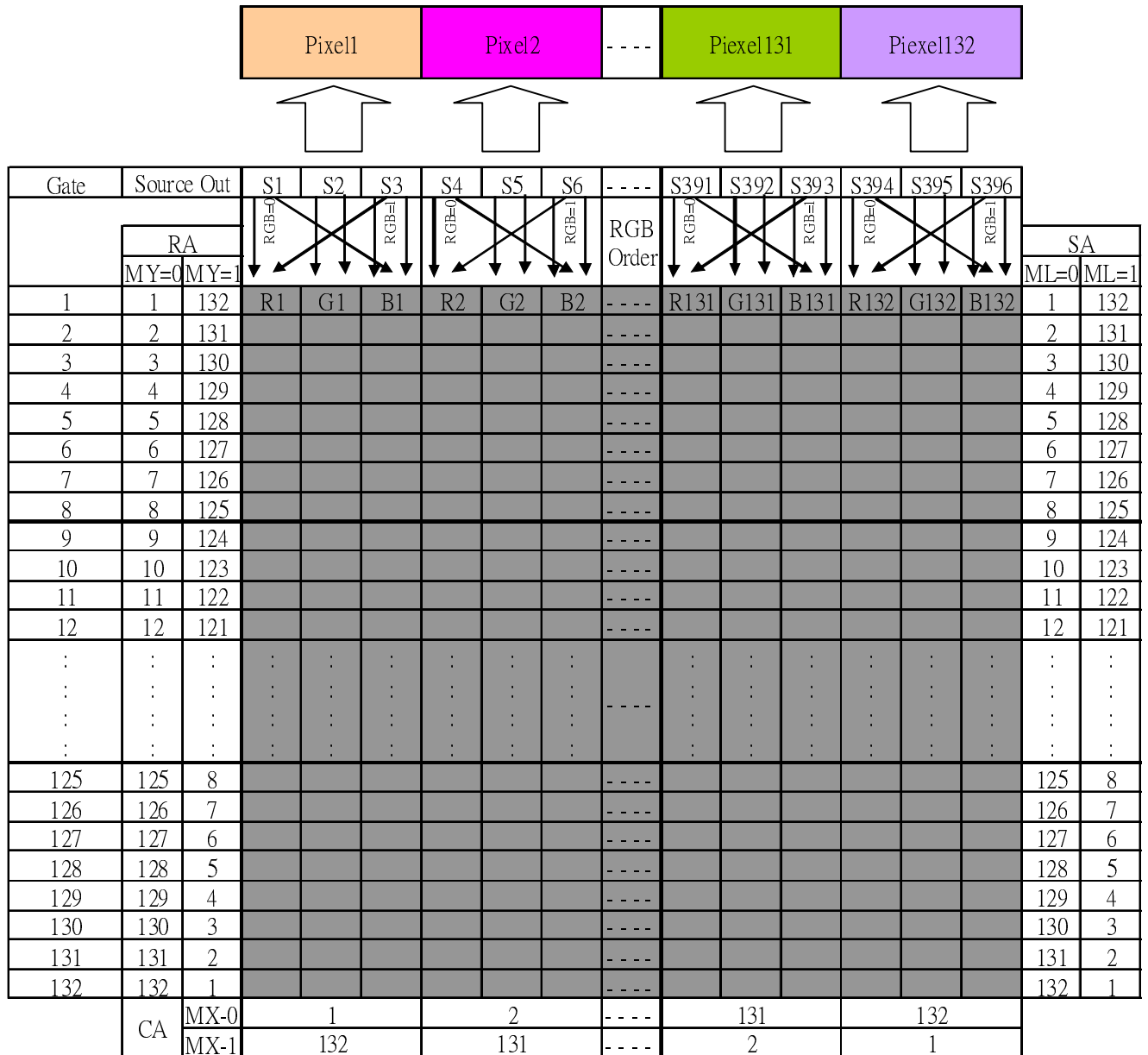
The display data RAM stores display dots and consists of 384,504 bits (132x18x162 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

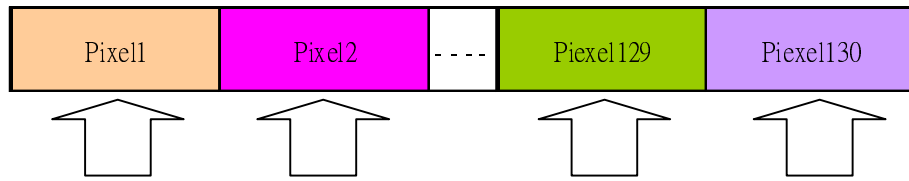


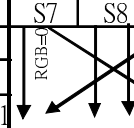
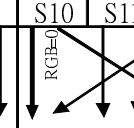
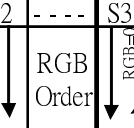
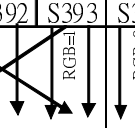
## 7.2 Memory to Display Address Mapping

### 7.2.1 132RGB x 132 resolution (GM[2:0] = "101", SMX=SMY=SRGB='0')

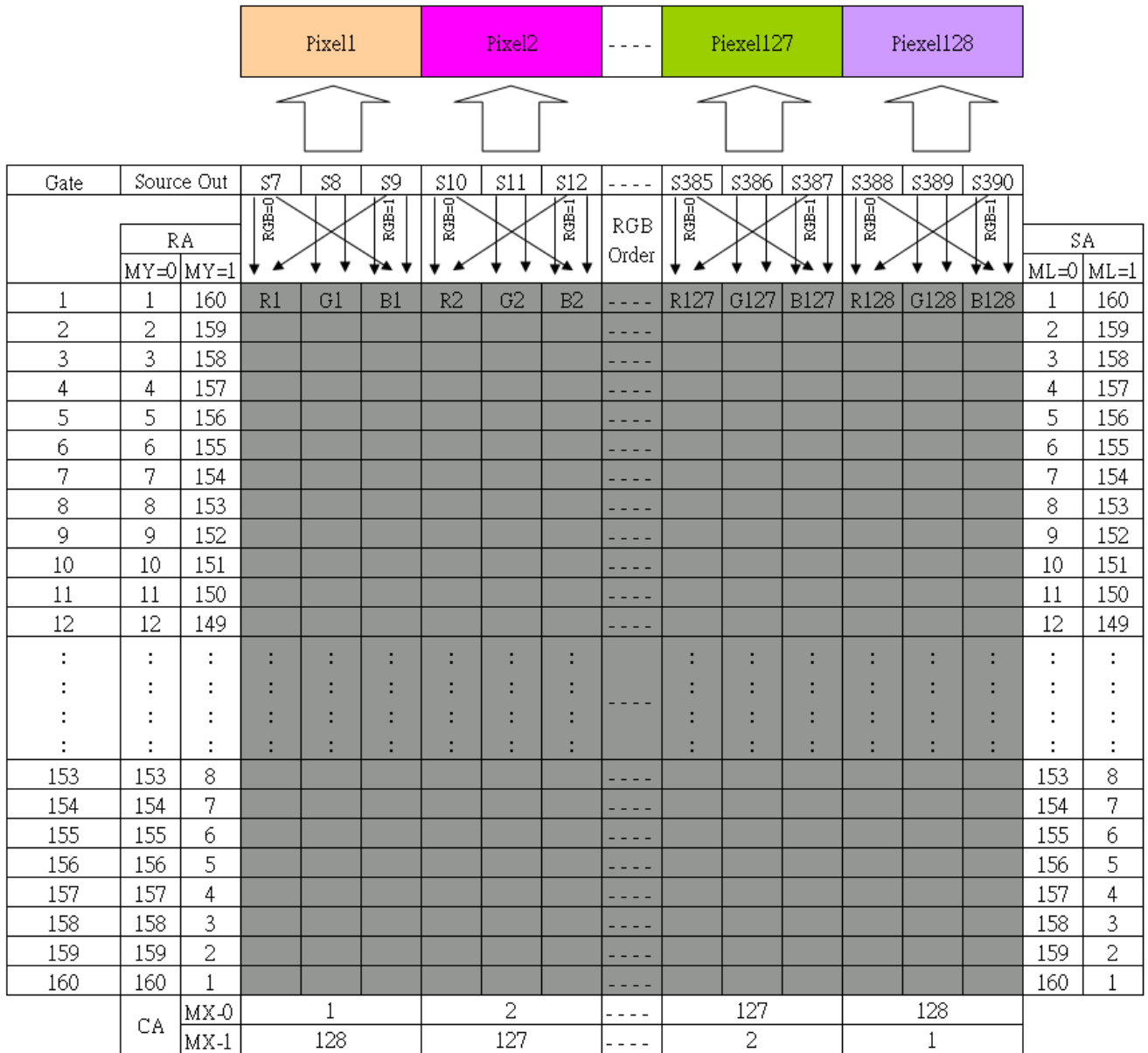


## 7.2.2 130RGB x 130 resolution(GM[2:0] = "100", SMX=SMY=SRGB='0')



Gate	Source Out		S7	S8	S9	S10	S11	S12	----	S391	S392	S393	S394	S395	S396		
	RA	MY=0MY=1					RGB Order									SA	
																ML=0ML=1	
1	1	130	R1	G1	B1	R2	G2	B2	----	R129	G129	B129	R130	G130	B130	1	130
2	2	129							----							2	129
3	3	128							----							3	128
4	4	127							----							4	127
5	5	126							----							5	126
6	6	125							----							6	125
7	7	124							----							7	124
8	8	123							----							8	123
9	9	122							----							9	122
10	10	121							----							10	121
11	11	120							----							11	120
12	12	119							----							12	119
:	:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	----	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
123	123	8							----							123	8
124	124	7							----							124	7
125	125	6							----							125	6
126	126	5							----							126	5
127	127	4							----							127	4
128	128	3							----							128	3
129	129	2							----							129	2
130	130	1							----							130	1
	CA	MX-0	1			2			----	129			130				
		MX-1	130			129			----	2			1				

### 7.2.3 128RGB x 160 resolution (GM[2:0] = "011", SMX=SMY=SRGB='0')



Note

RA = Row Address

CA = Column Address

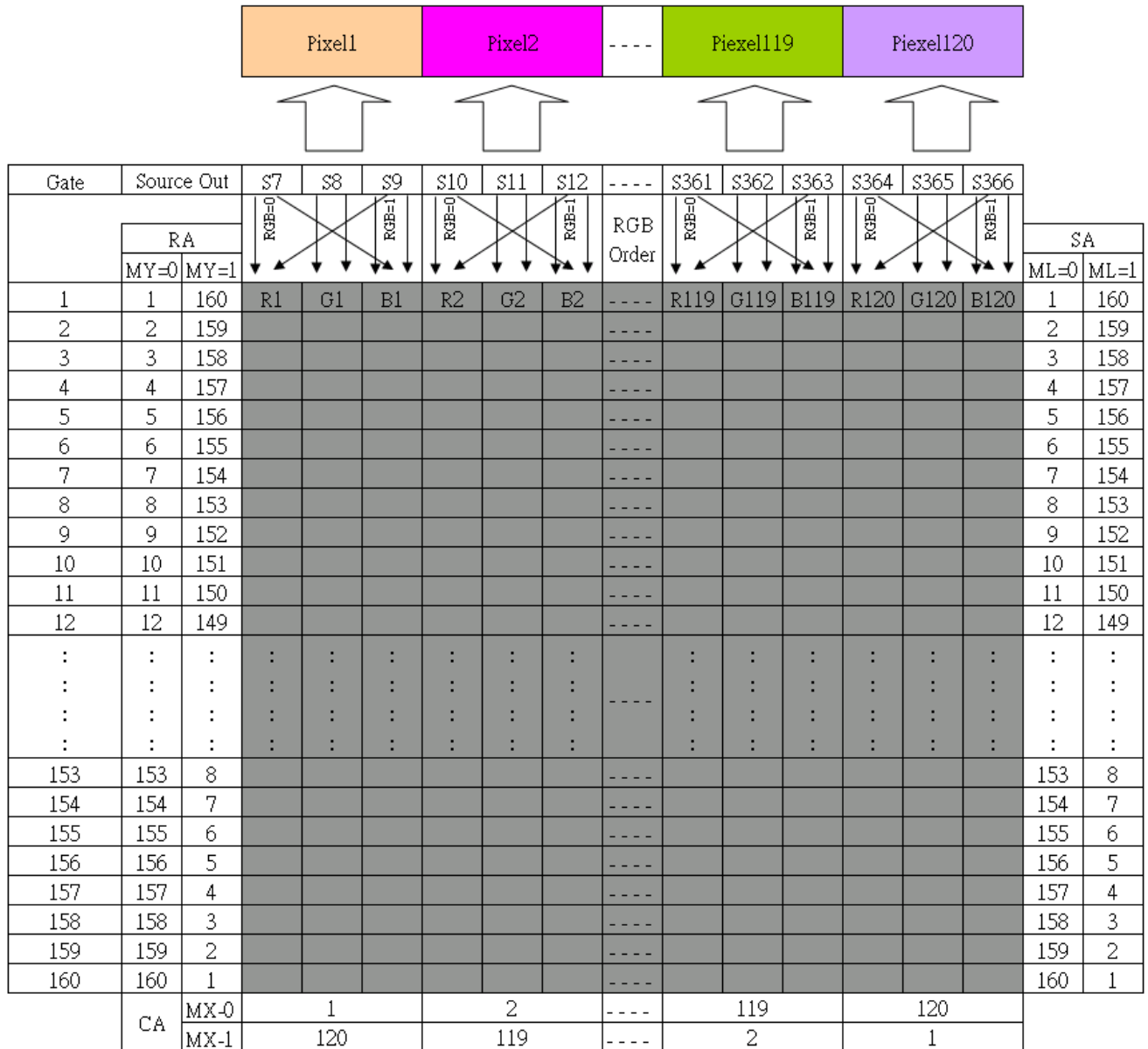
SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

## 7.2.4 120RGB x 160 resolution (GM[2:0] = "010", SMX=SMY=SRGB='0')



### Note

RA = Row Address

CA = Column Address

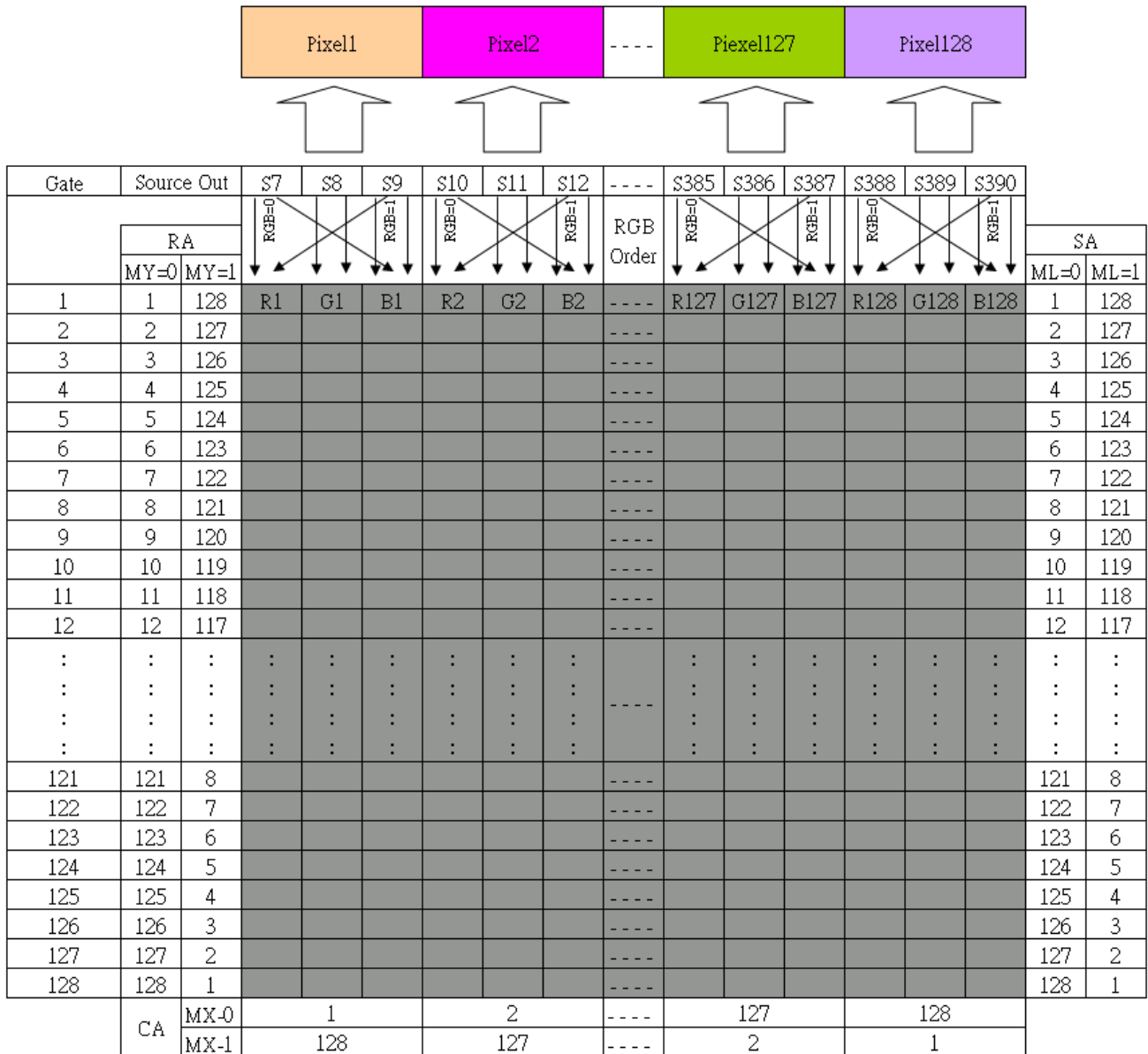
SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

## 7.2.5 128RGB x 128 resolution (GM[2:0] = "001", SMX=SMY=SRGB='0')



Note

RA = Row Address

CA = Column Address

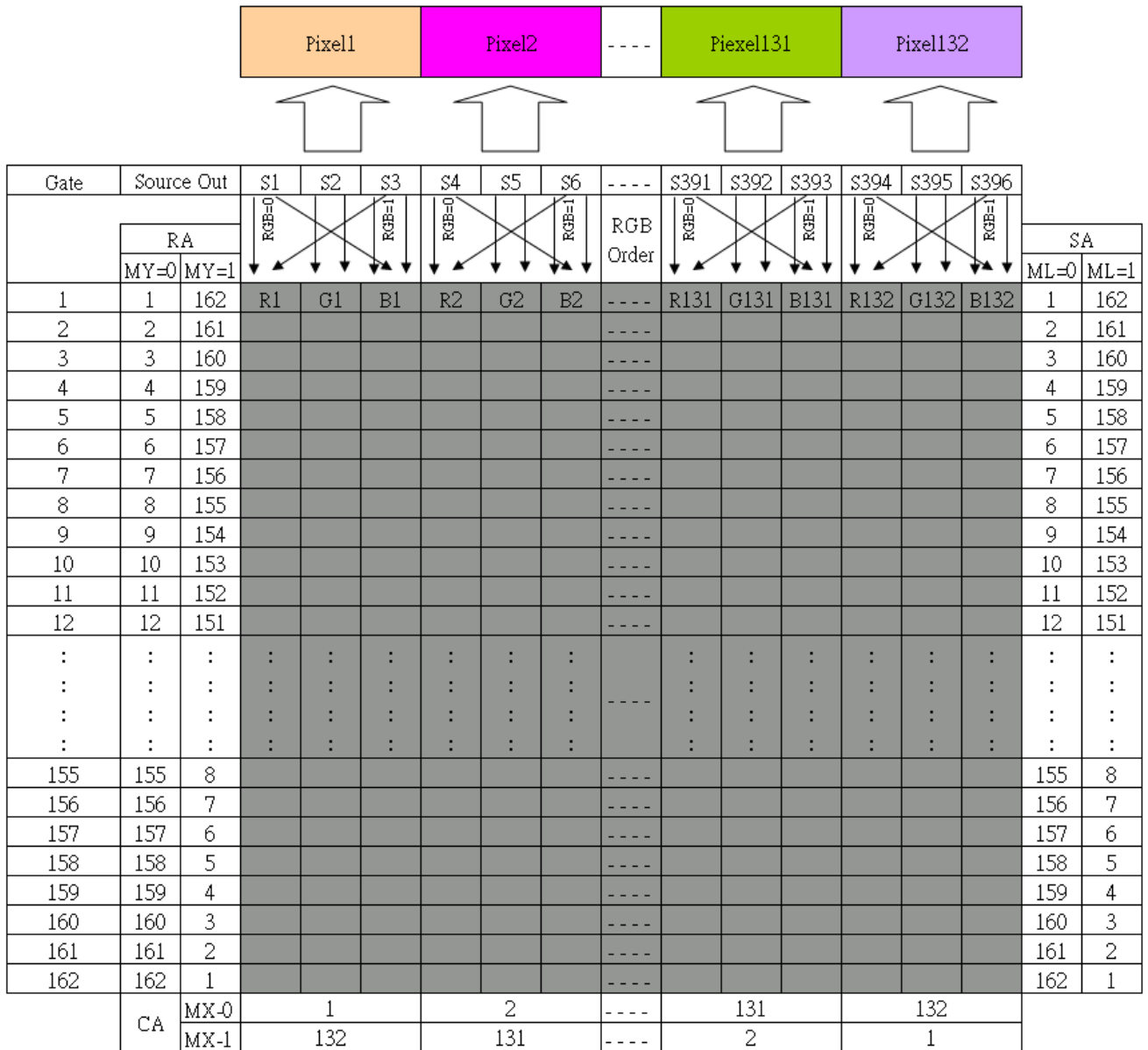
SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

## 7.2.6 132RGB x 162 resolution (GM[2:0] = "000", SMX=SMY=SRGB='0')



### Note

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

### 7.3 MCU to memory write/read direction (Address Counter)

The address counter set the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected(RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. When GM=011, 132RGB x 162, the address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command register XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0(0h) YS=0(0h) and XE=131(83h), YE=161(A1h)

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address(X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS)

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR", define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Below table shows the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image orientation, the controls for the column and page counters apply as below: -

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than "End Column(XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row(YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

Figure40: Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange	1	1	0		
XY Exchange Y-Mirror	1	1	1		

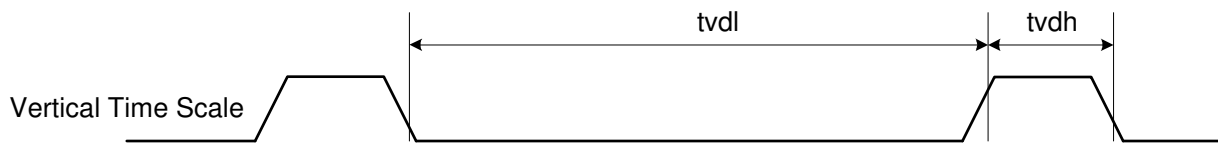
## 8. Tearing Effect Output Line

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

### 8.1 Tearing Effect Line Modes

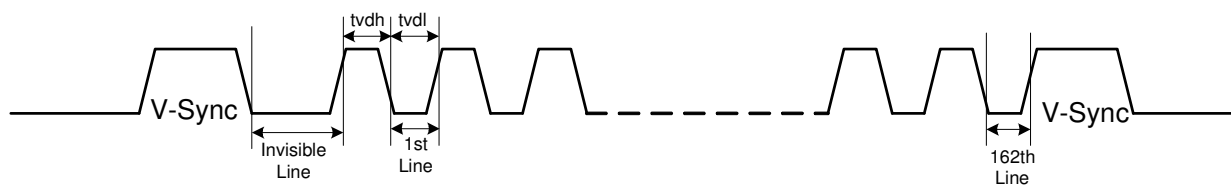
**Mode 1**, the Tearing Effect Output signal consists of V-Sync information only:



$t_{vdh}$  = The LCD display is not updated from the Frame Memory.

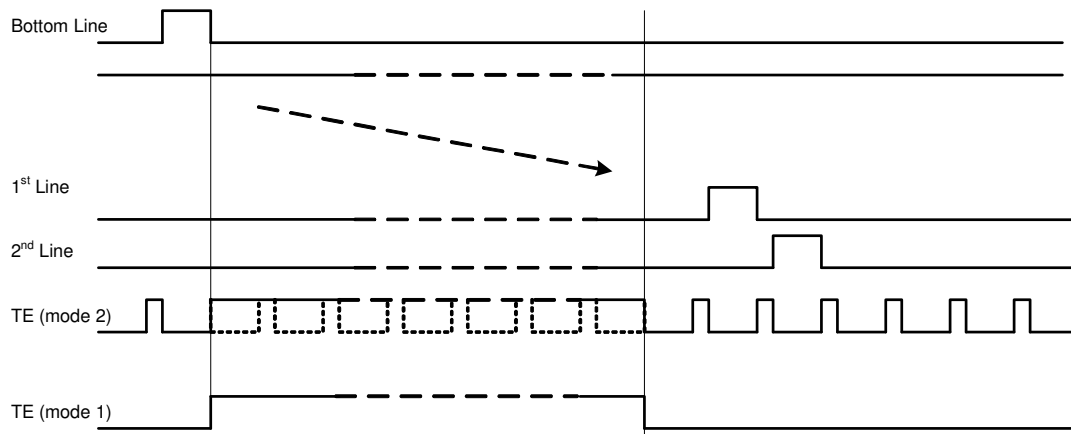
$t_{vdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

**Mode 2**, the Tearing Effect Output signal consists of V-Sync and H-Sync information, There is one V-sync and 162 H-sync pulses per field:



$t_{hdh}$  = The LCD display is not updated from the Frame Memory.

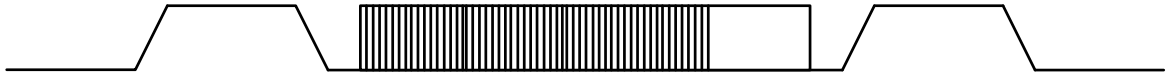
$T_{hdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



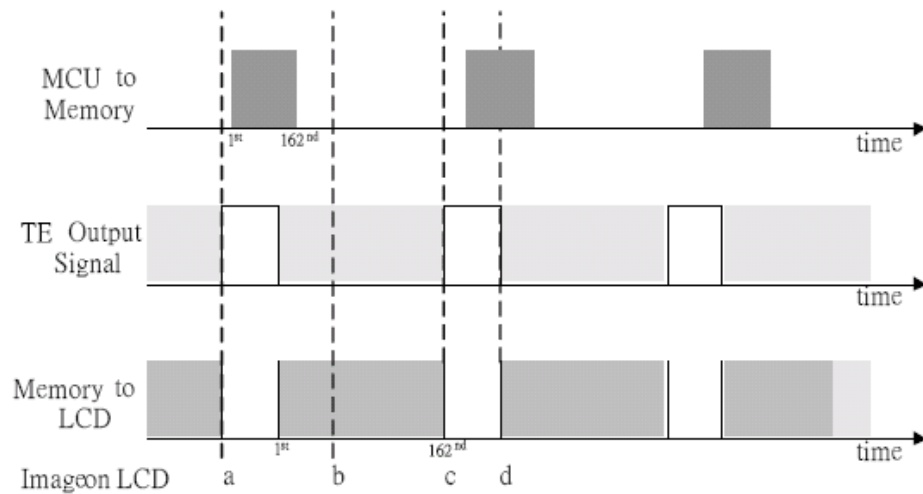
Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

## 8.2 Tearing Effect Line Timing

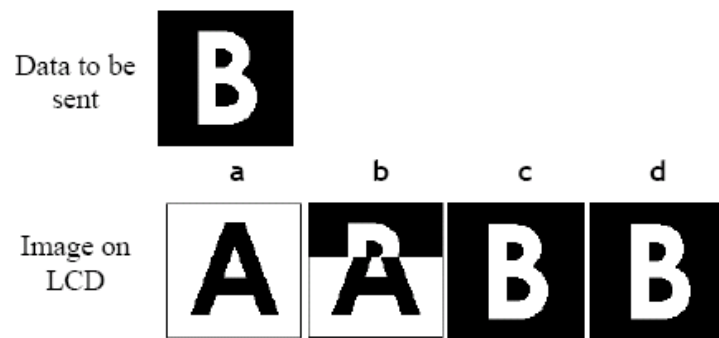
The Tearing Effect signal is described below:



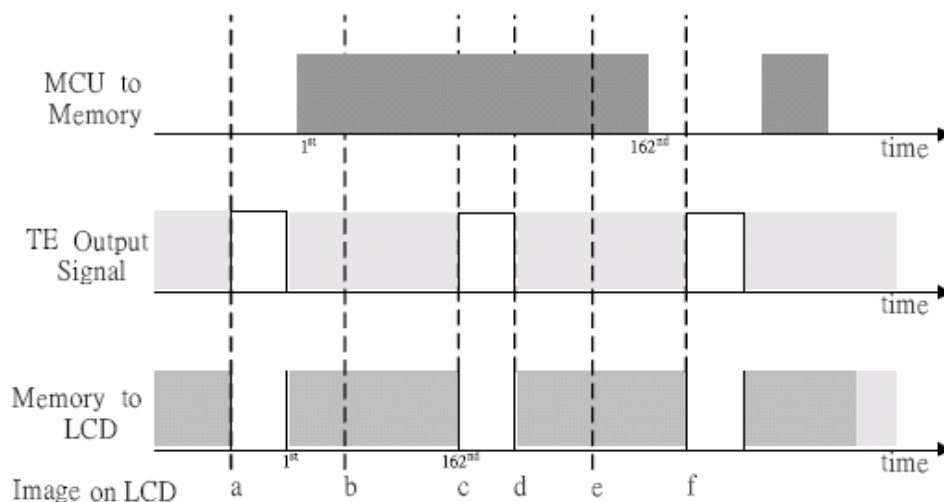
### 8.2.1 Example 1 MCU Write is Faster than Panel Read



Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

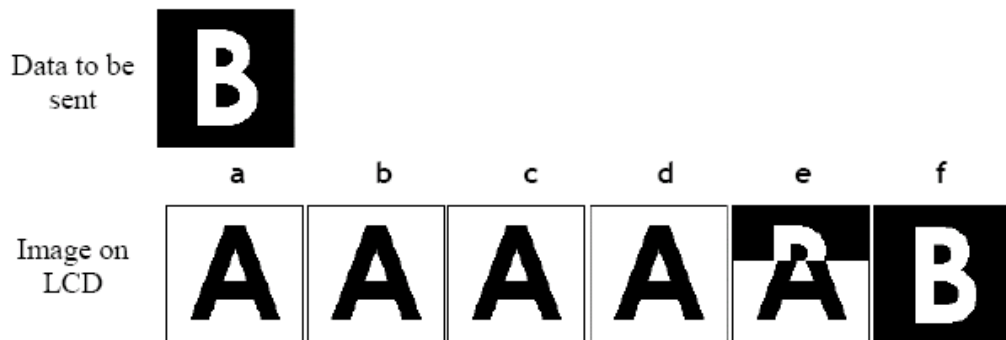


### 8.2.2 Example 2 MCU Write is slower than Panel Read



The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync

pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.



## 9. Power ON/OFF Sequence

VDDI and VPNL can be applied in any order.

VPNL and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VPNL and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VPNL can be powered down minimum 0msec after RESX has been released.

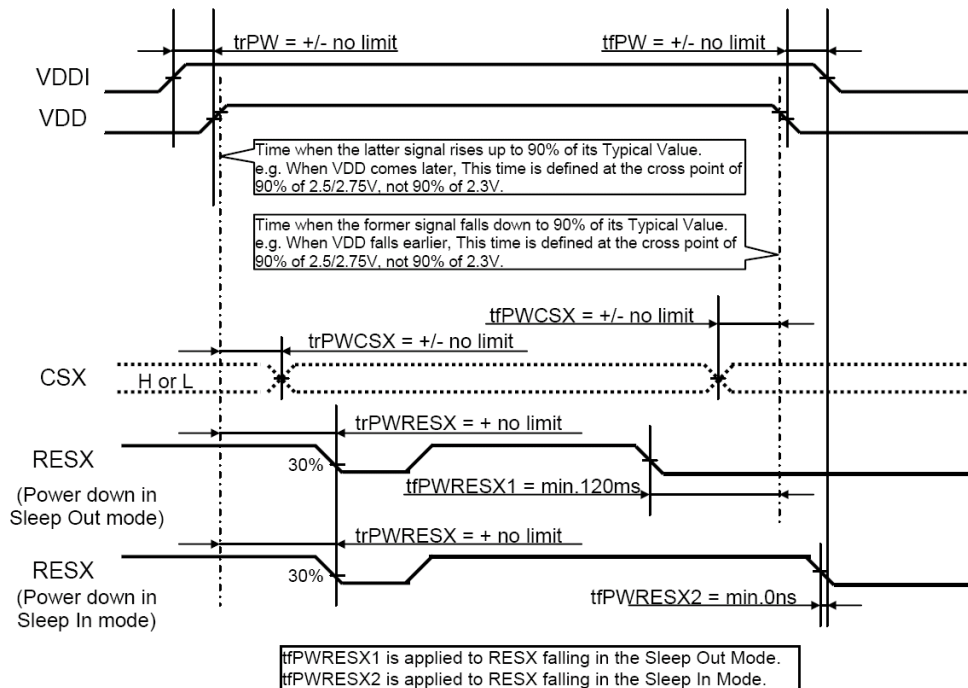
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Notes:

1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

### 9.1 Case 1 – RESX line is held high or Unstable by Host at Power –On

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VPNL and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

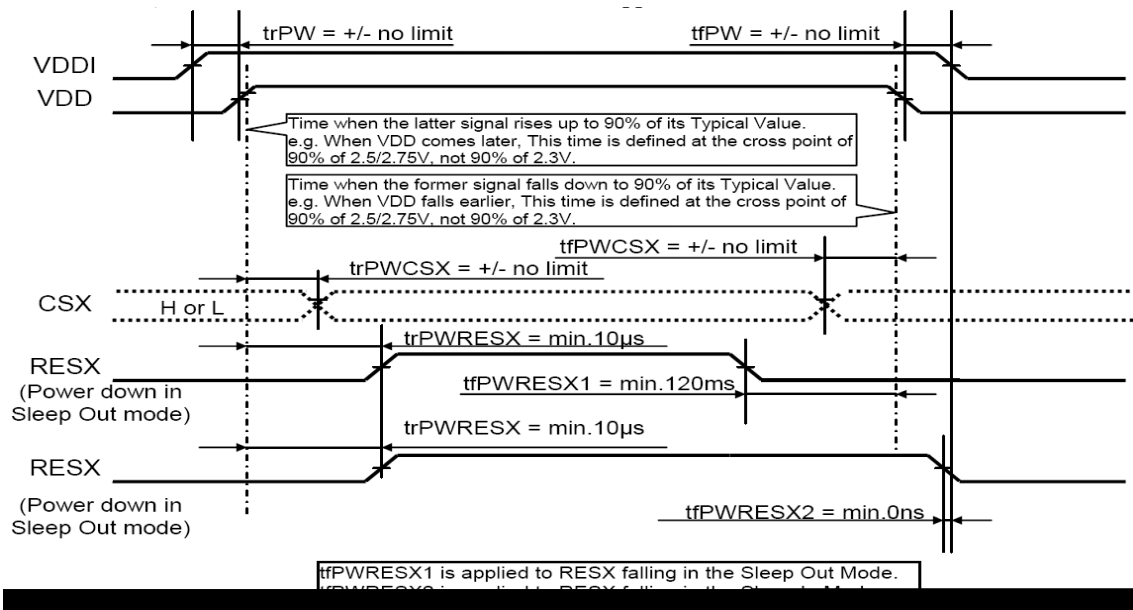


Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

### 9.2 Case 2 – RESX line is held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum

10 sec after both VPNL and VDDI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

### 9.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. The display module must meet following requirements:

1. There cannot be any damages for the display module or the display module cannot cause any damages for the host or lines of the interface.
2. There cannot be any abnormal visible effects (= Display must be blank) within 1 second on the display and remains blank until "Power On Sequence" powers it up.

## 10. Power Level Definition

### 10.1 Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

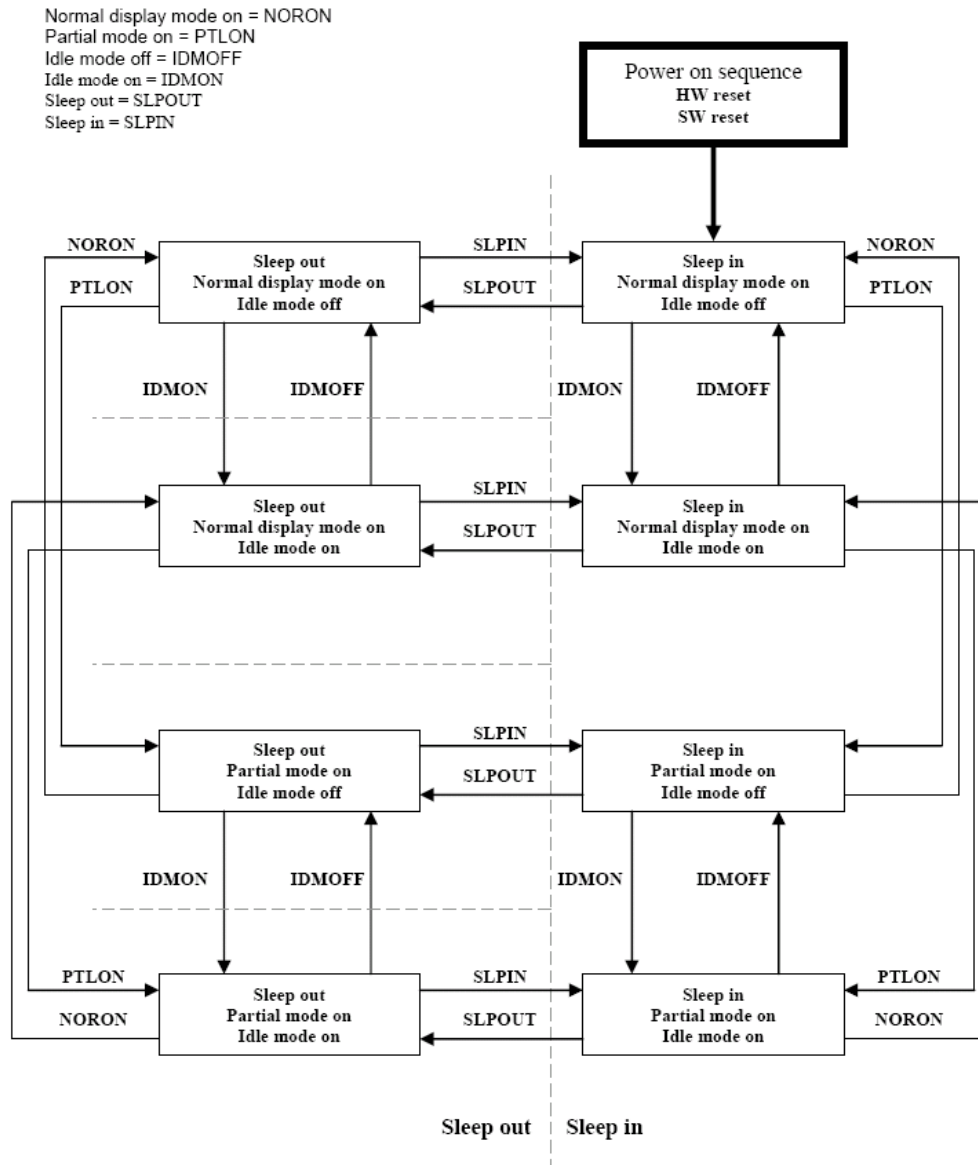
In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode.

In this mode, both VPNL and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

## 10.2 Power Flow Chart

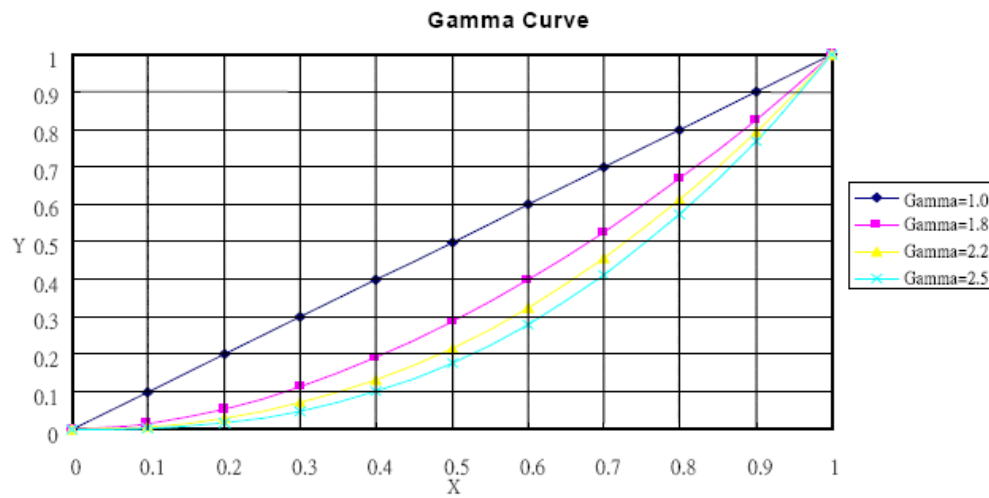


Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.

Note 3: It is recommended that it should be enter Sleep in before power off.

## 11. Gamma Curves



## 12. Reset

### 12.1 Registers

The registers that are initialized are listed below.

**Reset Table (Default Value, GM=000, 128RGB x 160)**

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	007Fh	007Fh	007Fh(127d) (when MV=0) 009Fh(159d) (when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	009Fh	009Fh	009Fh(159d) (when MV=0) 007Fh(127d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	009Fh	009Fh	009Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10 s after both VPNL & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=010, 120RGB x 160)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	0077h	0077h	0077h(119d) (when MV=0) 0077h(159d) (when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	009Fh	009Fh	009Fh(159d) (when MV=0) 0077h(119d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	009Fh	009Fh	009Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10 s after both VPNL & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=010, 128RGB x 128)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	007Fh	007Fh	007Fh(127d) (when MV=0) 0077h(127d) (when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	007Fh	007Fh	007Fh(127d) (when MV=0) 007Fh(127d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	007Fh	007Fh	007Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	0080h	0080h	0080h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10 s after both VPNL & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=011, 132RGB x 162)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	0083h	0083h	0083h(131d) (when MV=0) 00A1h(161d) (when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	00A1h	00A1h	00A1h(161d) (when MV=0) 0083h(131d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	00A1h	00A1h	00A1h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Line (TFE)	0000h	0000h	0000h

Reset Table (Default Value, GM=100, 130RGB x 130)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	0081h	0081h	0081h(when MV=0) 0081h(when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	0081h	0081h	0081h(when MV=0) 0081h(when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	0081h	0081h	0081h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	0082h	0082h	0082h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10 s after both VPNL & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=101, 132RGB x 132)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	0083h	0083h	0083h(when MV=0) 0083h(when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	0083h	0083h	0083h(when MV=0) 0083h(when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	0083h	0083h	0083h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	0084h	0084h	0084h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10 s after both VPINL & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

## 12.2 Input/Output Pins

### 12.2.1 Output Pins, I/O Pins

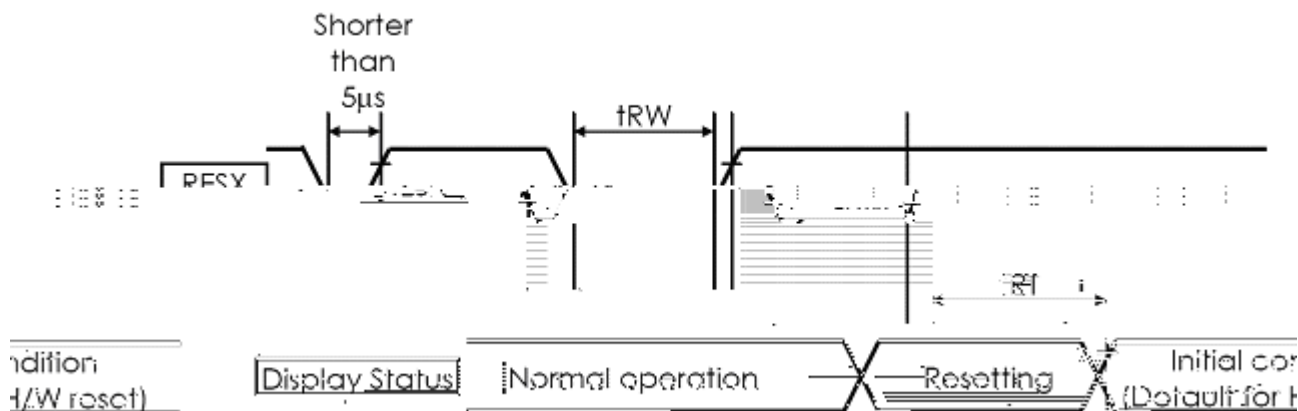
Output or Bi-direction pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17to D0(Output driver)	High-Z(Inactive)	High-Z(Inactive)	High-Z(Inactive)

Note: There will be no output from D[7..0] and SDA during Power On/Off sequences, Hardware Reset and Software Reset.

## 12.2.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	TBD	Input invalid	Input invalid	Input invalid	?
CSX	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
D/CX	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
WRX	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
RDX	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
D17 to D0	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
SDA	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid

## 12.3 Reset Timing



(VSS=0V, VDDI=1.65V to 1.95V, VPNL=2.6V to 2.9V, Ta = -30 to 70°C)

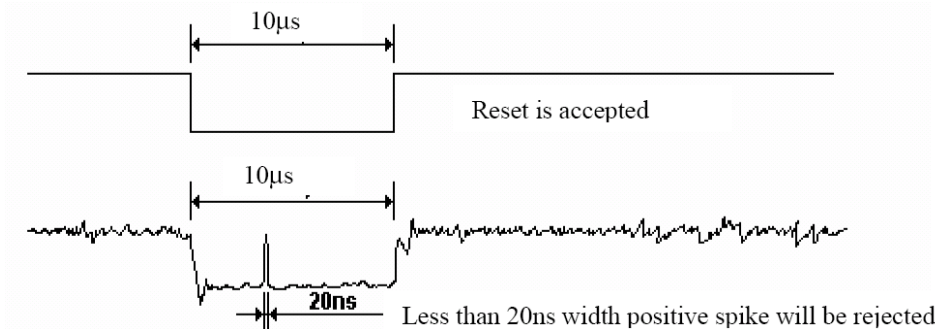
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	s
tREST	*2) Reset complete width	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Note

1. Spike due to an electrostatic discharge on RESX line does not cause system reset according to the table below.

RESX Pulse	Action
Shorten than 5 s	Reset Rejected
Longer than 10 s	Reset
Between 5 s and 10 s	Reset starts (It depends on voltage and temperature condtion.)

- During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for Hardware Reset.
- During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time ( $t_{REST}$ ) within 5ms after a rising edge of RESX.
- Spike Rejection also applies during a valid reset pulse as shown below:



- It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

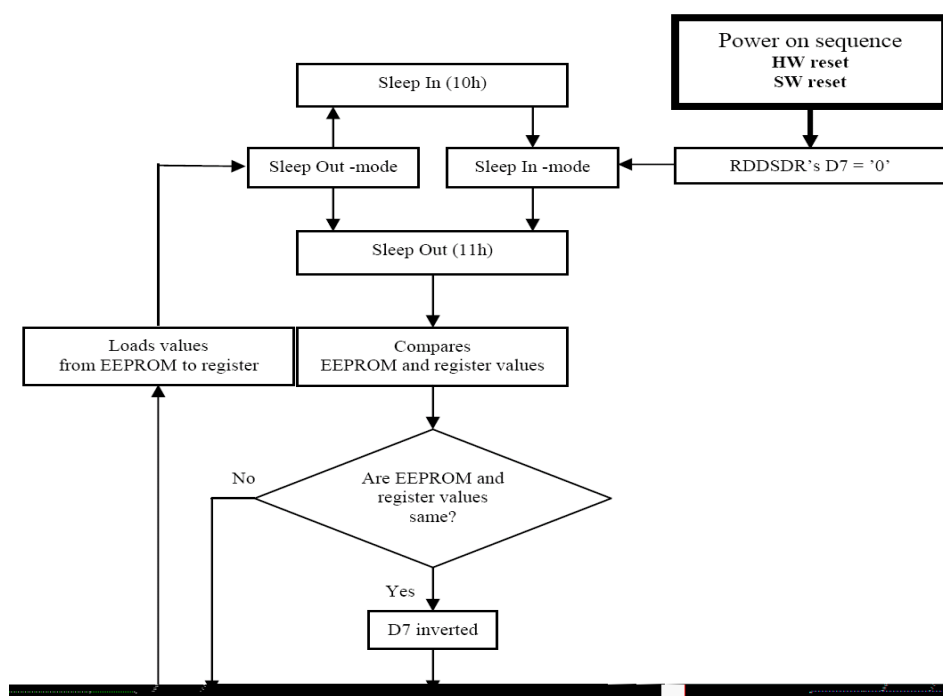
## 13. SleepOut – Command and Self-Diagnostic Functions of Display

### 13.1 Register loading Detection

Sleep Out-command (See section 16.1.2.12 Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command 16.1.2.10 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, the bit(D7) is not inverted (= increased by 1)

The flow chart for this internal function is following:



Note:

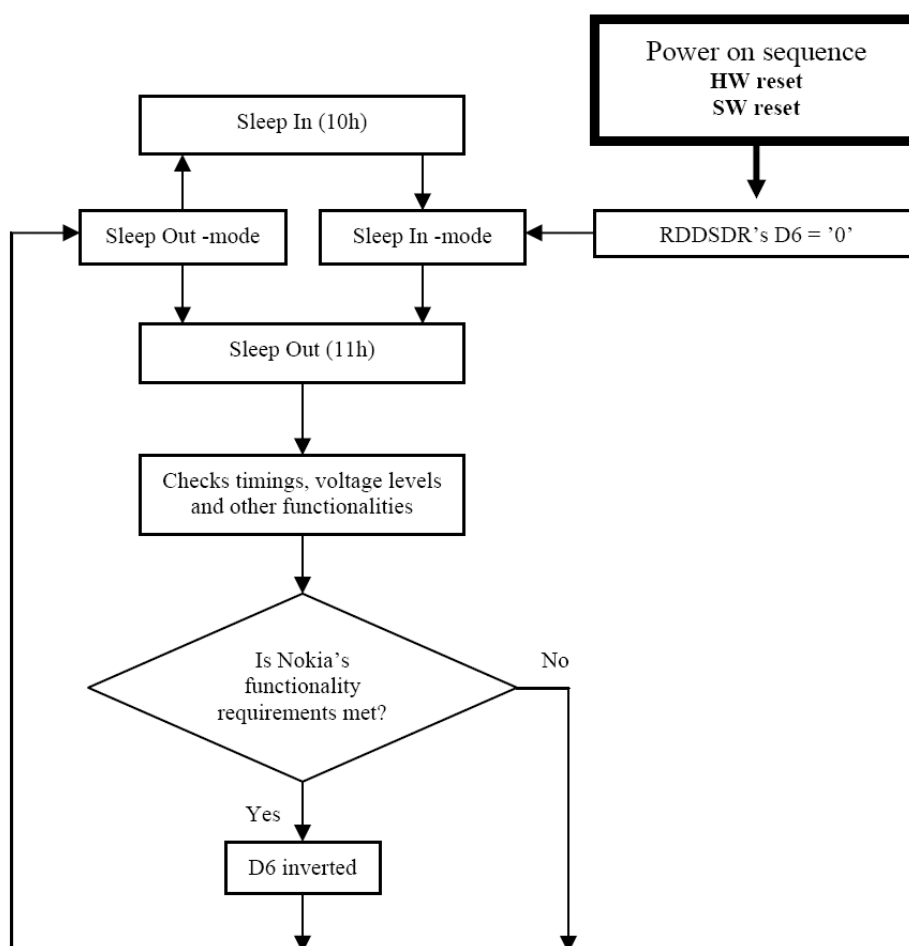
There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

## 13.2 Functionality Detection

Sleep Out-command (See section 16.1.2.12 Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 16.1.2.10 "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (=increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out –command, when there is changing from Sleep In –mode to Sleep Out –mode, before there is possible to check if Nokia's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out –mode.

## 14. Command

### 14.1 Command List

Code	Command	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Ref.
00H	<b>NOP</b> (No Operation)	X	0	0	0	0	0	0	0	0	00h	14.2.1
01H	<b>Software Reset</b>	X	0	0	0	0	0	0	0	1	01h	14.2.2
04H	<b>Read Display Identification Information</b>	X	0	0	0	0	0	1	0	0	04h	14.2.3
	1 <sup>st</sup> Parameter	X	X	X	X	X	X	X	X	X	X	
	2 <sup>nd</sup> Parameter	X	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	54h	
	3 <sup>rd</sup> Parameter	X	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h	
	4 <sup>th</sup> Parameter	X	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	66h	
09H	<b>Read Display Status</b>	X	0	0	0	0	1	0	0	1	09h	14.2.4
	1 <sup>st</sup> Parameter	X	X	X	X	X	X	X	X	X	X	
	2 <sup>nd</sup> Parameter	X	BSTON	MY	MX	MV	ML	RGB	MH	ST24	00h	
	3 <sup>rd</sup> Parameter	X	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	61h	
	4 <sup>th</sup> Parameter	X	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	00h	
	5 <sup>th</sup> Parameter	X	GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	00h	
0AH	<b>Read Display Power Mode</b>	X	0	0	0	0	1	0	1	0	0Ah	12.4.5
	1 <sup>st</sup> Parameter	X	X	X	X	X	X	X	X	X	X	
	2 <sup>nd</sup> Parameter	X	BSTON	IDMON	PLTON	SLPOUT	NORON	DISON	D1	D0	08h	
0BH	<b>Read Display MADCTL</b>	X	0	0	0	0	1	0	1	1	0Bh	12.4.6
	1 <sup>st</sup> Parameter	X	X	X	X	X	X	X	X	X	X	
	2 <sup>nd</sup> Parameter	X	MY	MX	MV	ML	RGB	MH	D1	D0	00h	
0CH	<b>Read Display Pixel Format</b>	X	0	0	0	0	1	1	0	0	0Ch	12.4.7
	1 <sup>st</sup> Parameter	X	X	X	X	X	X	X	X	X	X	
	2 <sup>nd</sup> Parameter	X	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	06h	
0DH	<b>Read Display Image Mode</b>	X	0	0	0	0	1	1	0	1	0Dh	12.4.8
	1 <sup>st</sup> Parameter	X	X	X	X	X	X	X	X	X	X	
	2 <sup>nd</sup> Parameter	X	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	00h	
0EH	<b>Read Display Signal Mode</b>	x	0	0	0	0	1	1	1	0	0Eh	14.2.9
	1 <sup>st</sup> Parameter	x	x	x	x	x	x	x	x	x	x	
	2 <sup>nd</sup> Parameter	x	D7	D6	HSON	VSON	PCKON	DEON	D1	D0	00h	
0FH	<b>Read Display Signal Mode</b>	x	0	0	0	0	1	1	1	1	0Fh	14.2.10
	1 <sup>st</sup> Parameter	x	X	x	x	x	x	x	x	x	x	
	2 <sup>nd</sup> Parameter	x	RELD	FUND	D5	D4	D3	D2	D1	D0	00h	

10H	Sleep In	x	0	0	0	1	0	0	0	0	10h	14.2.11
11H	Sleep Out	x	0	0	0	1	0	0	0	1	11h	14.2.12
12H	Partial Mode On	x	0	0	0	1	0	0	1	0	12h	14.2.13
13H	Normal Display Mode On	x	0	0	0	1	0	0	1	1	13h	14.2.14
20H	Display Inversion Off	x	0	0	1	0	0	0	0	0	20h	14.2.15
21H	Display Inversion On	x	0	0	1	0	0	0	0	1	21h	14.2.16
26H	Gamma Set	x	0	0	1	0	0	1	1	0	26h	14.2.17
	1 <sup>st</sup> Parameter	x	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h	
28H	Display Off	x	0	0	1	0	1	0	0	0	28h	14.2.18
29H	Display On	x	0	0	1	0	1	0	0	1	29h	14.2.19
2AH	Column Address Set	x	0	0	1	0	1	0	1	0	2Ah	14.2.20
	1 <sup>st</sup> Parameter	x	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-	
	2 <sup>nd</sup> Parameter	x	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	
	3 <sup>rd</sup> Parameter	x	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-	
	4 <sup>th</sup> Parameter	x	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-	
2BH	Page Address Set	x	0	0	1	0	1	0	1	1	2Bh	14.2.21
	1 <sup>st</sup> Parameter	x	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-	
	2 <sup>nd</sup> Parameter	x	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	
	3 <sup>rd</sup> Parameter	x	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-	
	4 <sup>th</sup> Parameter	x	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-	
2CH	Memory Write	x	0	0	1	0	1	1	0	0	2Ch	14.2.22
	1 <sup>st</sup> Parameter	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-	
	:	x	:	:	:	:	:	:	:	:	:	
	N <sup>th</sup> Parameter	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-	
2DH	Color Setting for 4K, 65K and 262K	x	0	0	1	0	1	1	0	1	2Dh	14.2.23
	1 <sup>st</sup> Parameter	x	x	x	R005	R004	R003	R002	R001	R000	-	
	:	x	x	x	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-	
	32 <sup>nd</sup> parameter	x	x	x	R315	R314	R313	R312	R311	R310	-	
	33 <sup>rd</sup> Parameter	x	x	x	G005	G004	G003	G002	G001	G000	-	
	:	x	x	x	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-	
	96 <sup>th</sup> Parameter	x	x	x	G635	G634	G633	G632	G631	G630	-	
	97 <sup>th</sup> Parameter	x	x	x	B005	B004	B003	B002	B001	B000	-	
	:	x	x	x	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-	
	128 <sup>th</sup> Parameter	x	x	x	B315	B314	B313	B312	B311	B310	-	

<b>2EH</b>	<b>Memory Read</b>	x	0	0	1	0	1	1	1	0	2Eh	14.2.24
	1 <sup>st</sup> Parameter	x	x	x	x	x	x	x	x	x	-	
	2 <sup>nd</sup> Parameter	x	D17	D16	D15	D14	D13	D12	D11	D10	-	
	:	x	:	:	:	:	:	:	:	:	-	
	N <sup>th</sup> Parameter	x	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	
<b>30H</b>	<b>Partial Area</b>	x	0	0	1	1	0	0	0	0	30h	14.2.25
	1 <sup>st</sup> Parameter	x	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-	
	2 <sup>nd</sup> Parameter	x	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	
	3 <sup>rd</sup> Parameter	x	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-	
	4 <sup>th</sup> Parameter	x	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-	
<b>33H</b>	<b>Vertical Scrolling Definition</b>	x	0	0	1	1	0	0	1	1	33h	14.2.26
	1 <sup>st</sup> Parameter	x	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-	
	2 <sup>nd</sup> Parameter	x	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-	
	3 <sup>rd</sup> Parameter	x	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-	
	4 <sup>th</sup> Parameter	x	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-	
	5 <sup>th</sup> Parameter	x	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-	
	6 <sup>th</sup> Parameter	x	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-	
<b>34H</b>	<b>Tearing Effect Line Off</b>	x	0	0	1	1	0	1	0	0	34h	14.2.27
<b>35H</b>	<b>Tearing Effect Line On</b>	x	0	0	1	1	0	1	0	1	35h	14.2.28
	1 <sup>st</sup> Parameter	x	x	x	x	x	x	x	x	M	00h	
<b>36H</b>	<b>Memory Access Control</b>	x	0	0	1	1	0	1	1	0	36h	14.2.29
	1 <sup>st</sup> Parameter	x	MY	MX	MV	ML	RGB	MH	x	x	00h	
<b>37H</b>	<b>Vertical Scrolling Start Address</b>	x	0	0	1	1	0	1	1	1	37h	14.2.30
	1 <sup>st</sup> Parameter	x	SSA 15	SSA 14	SSA 13	SSA 12	SSA 11	SSA 10	SSA 9	SSA 8	00h	
	2 <sup>nd</sup> Parameter	x	SSA 7	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	00h	
<b>38H</b>	<b>Idle Mode Off</b>	x	0	0	1	1	1	0	0	0	38h	14.2.31
<b>39H</b>	<b>Idle Mode On</b>	x	0	0	1	1	1	0	0	1	39h	14.2.32
<b>3AH</b>	<b>Interface Pixel Format</b>	x	0	0	1	1	1	0	1	0	3Ah	14.2.33
	1 <sup>st</sup> Parameter	x	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h	

B1H	Frame Rate Control (In normal mode/Full colors)		1	0	1	1	0	0	0	1	B1h	14.2.37
	1 <sup>st</sup> Parameter		x	x	x	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	x	
	2 <sup>nd</sup> Parameter		x	x	VPA5	VPA4	VPA3	VPA2	VPA1	VPA0	x	
B2H	Frame Rate Control(In Idle mode/8-colors)		1	0	1	1	0	0	1	0	B2h	14.2.38
	1 <sup>st</sup> Parameter		x	x	x	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0	x	
	2 <sup>nd</sup> Parameter		x	x	VPB5	VPB4	VPB3	VPB2	VPB1	VPB0	x	
B3H	Frame Rate Control(In Partial mode/full colors)		1	0	1	1	0	0	1	1	B3h	14.2.39
	1 <sup>st</sup> Parameter		x	x	x	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0	x	
	2 <sup>nd</sup> Parameter		x	x	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	x	
B4H	Display Inversion Control	x	1	0	1	1	0	1	0	0	B4h	14.2.40
	1 <sup>st</sup> Parameter	x	0	0	0	0	0	NLA	NLB	NLC	02H	
B5H	RGB Interface Blanking Porch setting	x	1	0	1	1	0	1	0	1	B5h	14.2.41
	1 <sup>st</sup> Parameter	x	x	x	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	08h	
	2 <sup>nd</sup> Parameter	x	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	03h	
	3 <sup>rd</sup> Parameter	x	x	x	x	x	x	x	VBP9	VBP8	00h	
B6H	Display Function Set	x	1	0	1	1	0	1	1	0	B6h	14.2.41
	1 <sup>st</sup> Parameter		x	x	NO1	NO0	SDT1	SDT0	EQ1	EQ2	06h	
	2 <sup>nd</sup> Parameter		x	x	x	x	x	PTG0	PT1	PT0	02h	
B7H	Source Driver Direction Control	x	1	0	1	1	0	1	1	1	B7h	14.2.42
	1 <sup>st</sup> Parameter	x	0	0	0	0	0	0	0	CRL	00h	
B8H	Gate Driver Direction Control	x	1	0	1	1	1	0	0	0	B8h	14.2.43
	1 <sup>st</sup> Parameter	x	0	0	0	0	0	0	0	CTB	00h	
C0H	Power_Control1	x	1	1	0	0	0	0	0	0	C0h	14.2.44
	1 <sup>st</sup> Parameter	x	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	x	
	2 <sup>nd</sup> Parameter	x	0	0	0	0	0	VC2	VC1	VC0	02h	
C1H	Power_Control2	x	1	1	0	0	0	0	0	1	C1h	14.2.45
	1 <sup>st</sup> Parameter	x	0	0	0	0	0	BT2	BT1	BT0	07h	

C2H	Power_Control3	x	1	1	0	0	0	0	1	0	C2h	14.2.46
	1 <sup>st</sup> Parameter	x	0	0	0	0	0	APA2	APA1	APA0	00h	
C3H	Power_Control4	x	1	1	0	0	0	0	1	1	C3h	14.2.47
	1 <sup>st</sup> Parameter	x	0	0	0	0	0	APB2	APB1	APB0	00h	
C4H	Power_Control 5	x	1	1	0	0	0	1	0	0	C4h	14.2.48
	1 <sup>st</sup> Parameter	x	0	0	0	0	0	APC2	APC1	APC1	01h	
C5H	VCOM_Control 1	x	1	1	0	0	0	1	0	1	C5h	14.2.49
	1 <sup>st</sup> Parameter	x	x	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	-	
	2 <sup>nd</sup> Parameter	x	0	VML6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	-	
C6H	VCOM_Control 2	x	1	1	0	0	0	1	1	0	C6h	14.2.50
	1 <sup>st</sup> Parameter	x	0	0	VMA 5	VMA 4	VMA 3	VMA 2	VMA 1	VMA 0	13h /06 h	
C7H	VCOM Offset Control	x	1	1	0	0	0	1	1	1	C7h	14.2.51
	1 <sup>st</sup> Parameter	0	nVM*	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	40h	
D3H	Write ID4 Value	x	1	1	0	1	0	0	1	1	D3h	14.2.52
	1 <sup>st</sup> Parameter	x	x	x	x	x	x	x	x	x	x	
	2 <sup>nd</sup> Parameter	x	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	91h	
	3 <sup>rd</sup> Parameter	x	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	63h	
	4 <sup>th</sup> Parameter	x	x	x	x	x	ID433	ID432	ID431	ID430	00h	
	5 <sup>th</sup> Parameter	x	x	x	x	x	x	x	x	x	x	
D5H	NV Memory Function Controller(1)	x	1	1	0	1	1	0	1	0	D5h	14.2.53
	1 <sup>st</sup> Parameter	x	ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20	00h	
	2 <sup>nd</sup> Parameter	x	OTP_ BS	0	0	0	OTP_ VMF3	OTP_ VMF2	OTP_ VMF1	OTP_ VMF0	00h	
D6H	NV Memory Function Controller(2)	x	1	1	0	1	1	0	1	0	D6h	14.2.54
	1 <sup>st</sup> Parameter	x	OTP_ D[7]	OTP_D [6]	OTP_ D[5]	OTP_ D[4]	OTP_ D[3]	OTP_ D[2]	OTP_ D[1]	OTP_D [0]	00h	
	2 <sup>nd</sup> Parameter	x	0	0	0	0	0	0	OTP_ TP[1]	OTP_ TP[0]	00h	
D7H	NV Memory Function Controller(3)	x	1	1	0	1	1	0	1	0	D7h	14.2.55
	1 <sup>st</sup> Parameter	x	0	1	0	1	0	1	0	1	55h	
	2 <sup>nd</sup> Parameter	x	1	0	1	0	1	0	1	0	AAh	

	3 <sup>rd</sup> Parameter	x	0	1	1	0	0	1	1	0	66h	
DAH	Read ID1	x	1	1	0	1	1	0	1	0	DAh	14.2.34
	1 <sup>st</sup> Parameter	x	x	x	x	x	x	x	x	x	x	
	2 <sup>nd</sup> Parameter	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	54h	
DBH	Read ID2	x	1	1	0	1	1	0	1	1	DBh	14.2.35
	1 <sup>st</sup> Parameter	x	x	x	x	x	x	x	x	x	x	
	2 <sup>nd</sup> Parameter	x	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h	
DCH	Read ID3	x	1	1	0	1	1	1	0	0	DC h	14.2.36
	1 <sup>st</sup> Parameter	x	x	x	x	x	x	x	x	x	x	
	2 <sup>nd</sup> Parameter	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	66h	
E0H	Positive Gamma Correction Setting		1	1	1	0	0	0	0	0	E0h	14.2.57
	1 <sup>st</sup> Parameter		x	x	VP0[5:0]						-	
	2 <sup>nd</sup> Parameter		x	x	VP1[5:0]						-	
	3 <sup>rd</sup> Parameter		x	x	VP2[5:0]						-	
	4 <sup>th</sup> Parameter		x	x	VP4[5:0]						-	
	5 <sup>th</sup> Parameter		x	x	VP6[5:0]						-	
	6 <sup>th</sup> Parameter		x	x	x	VP13[4:0]					-	
	7 <sup>th</sup> Parameter		x	VP20[6:0]							-	
	8 <sup>th</sup> Parameter		VP36[3:0]				VP27[3:0]				-	
	9 <sup>th</sup> Parameter		x	VP43[6:0]							-	
	10 <sup>th</sup> Parameter		x	x	VP50[5:0]						-	
	11 <sup>st</sup> Parameter		x	x	VP57[5:0]						-	
	12 <sup>nd</sup> Parameter		x	x	VP59[5:0]						-	
	13 <sup>rd</sup> Parameter		x	x	VP61[5:0]						-	
	14 <sup>th</sup> Parameter		x	x	VP62[5:0]						-	
15 <sup>th</sup> Parameter		x	x	VP63[5:0]						-		
	Negative Gamma Correction Setting		1	1	1	0	0	0	0	1	E1h	
	1 <sup>st</sup> Parameter		x	x	VN63[5:0]						-	
	2 <sup>nd</sup> Parameter		x	x	VN62[5:0]						-	
	3 <sup>rd</sup> Parameter		x	x	VN61[5:0]						-	

	7 <sup>th</sup> Parameter		x	VN43[6:0]							-	
	8 <sup>th</sup> Parameter		VN27[3:0]			VN36[3:0]					-	
	9 <sup>th</sup> Parameter		x	VN20[6:0]							-	
	10 <sup>th</sup> Parameter		x	x	VN13[5:0]						-	
	11 <sup>st</sup> Parameter		x	x	VN6[5:0]						-	
	12 <sup>nd</sup> Parameter		x	x	VN4[5:0]						-	
	13 <sup>rd</sup> Parameter		x	x	VN2[5:0]						-	
	14 <sup>th</sup> Parameter		x	x	VN1[5:0]						-	
	15 <sup>th</sup> Parameter		x	x	VN0[5:0]						-	
E6H	Deep stand by control		1	1	1	0	0	1	1	0	E6h	
	1 <sup>st</sup> Parameter		x	x	x	x	x	x	x	DSTB	00h	
F2H	GAM_R_SEL		1	1	1	1	0	0	1	0	F2h	14.2.59
	1 <sup>st</sup> Parameter		x	x	x	x	x	x	x	GAM_R_SEL	Write	

## 14.2 Command Description

### 14.2.1 NOP (00h)

00H	NOP (No Operation)																								
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		X	0	0	0	0	0	0	0	0	00												
Parameter	NO PARAMETER																								
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.  X = Don't care.																								
Restriction	None																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	None																								

## 14.2.2 Software Reset (01h)

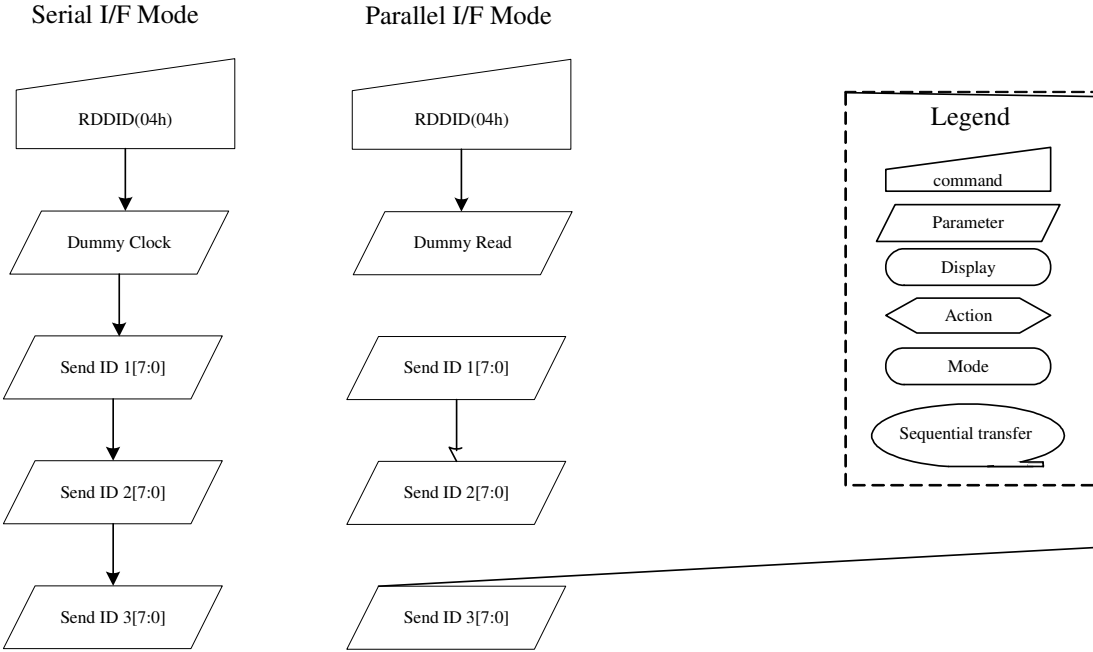
01H	SWRESET (Software Reset)																								
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		X	0	0	0	0	0	0	0	1	01												
Parameter	NO PARAMETER																								
Description	<p>When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>Note: The Frame Memory contents are affected by this command.</p> <p>X = Don't care</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	<div><div><div>SW RESET</div><div>↓</div><div>Display whole blank screen</div><div>↓</div><div>Set Commands to S/W Default Vaule</div><div>↓</div><div>Sleep in Mode</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								



a-Si TFT LCD Single Chip Driver  
132RGBx162 Resolution and 262K color

**ILI9163C**

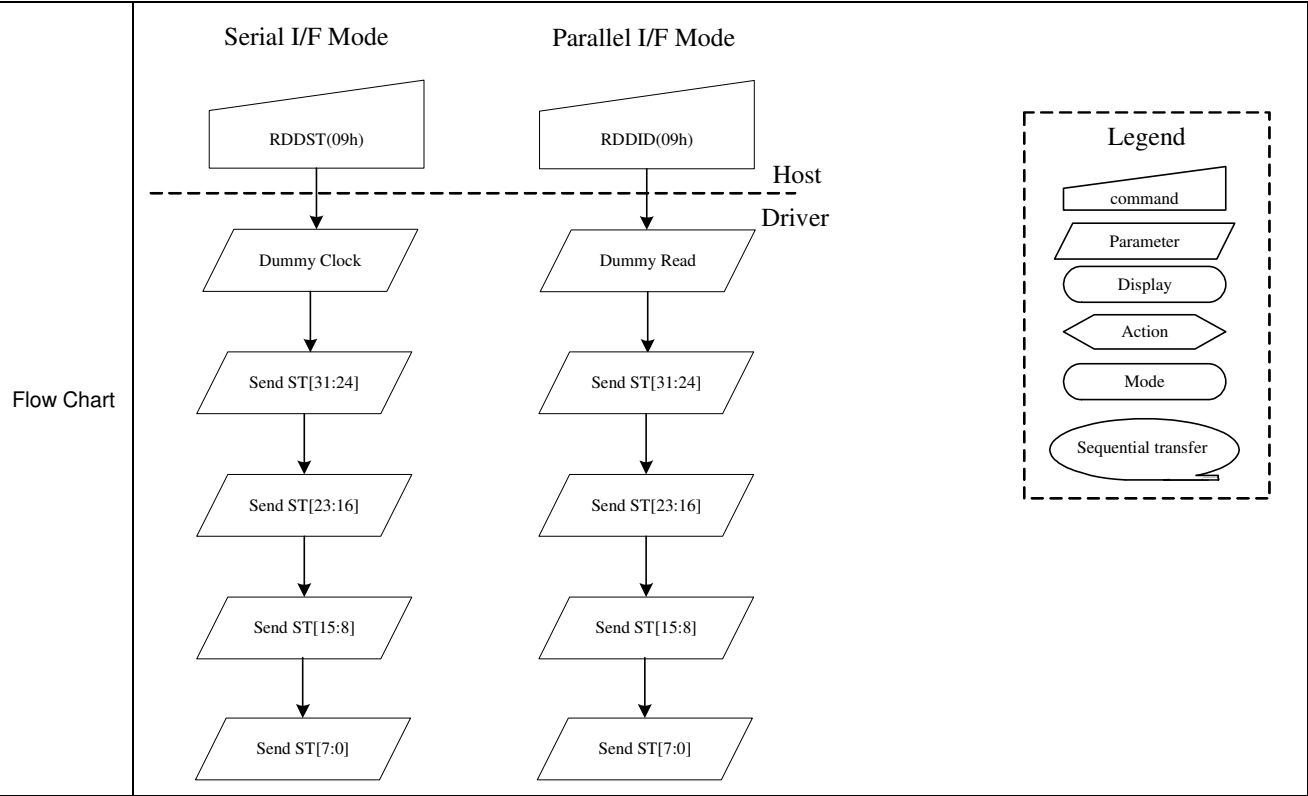
Flow Chart



#### 14.2.4 Read Display Status (09h)

09H	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	0	0	1	0	0	1	09h
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x
2 <sup>nd</sup> Parameter	1		1	x	BOTSON	MY	MX	MV	ML	RGB	MH	ST24	x
3 <sup>rd</sup> Parameter	1		1	x	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	x
4 <sup>th</sup> Parameter	1		1	x	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	x
5 <sup>th</sup> Parameter	1		1	x	GCS1	GCS0	TELOM	HSOON	VSON	PCKON	DEON	ST0	x
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description		Value									
	BSTON	Booster Voltage Status		"1"=Booster on,"0"=Booster off									
	MY	Row Address Order(MY)		"1"=Decrement, (Bottom to Top, when MADCTL(36h) D7='1') "0"=Increment, (Top to Bottom, when MADCTL(36h) D7='0')									
	MX	Column Address Order(MX)		"1"=Decrement, (Right to Left, when MADCTL(36h) D6='1') "0"=Increment, (Left to Right, when MADCTL(36h) D6='0')									
	MV	Row/Column Exchange(MV)		"1"=Row/column exchange, (when MADCTL (36h) D5='1') "0"=Normal (MV=0), (when MADCTL(36h)D5='0')									
	ML	Vertical refresh Order(ML)		"1"=Decrement, (LCD refresh Bottom to Top, when MADCTL(36h)D4='1') "0"=Increment, (LCD refresh Top to Bottom, when MADCTL(36h)D4='0')									
	RGB	RGB/BGR Order(RGB)		"1"=BGR,(When MADCTL(36h)D3='1') "0"=RGB,(When MADCTL(36h)D3='0')									
	MH	Horizontal refresh Order(MH)		"1"=Decrement, (LCD refresh Right to Left, when MADCTL(36h) D2='1') "0"=Increment, (LCD refresh Left to Right, when MADCTL(36h) D2='0')									
	ST24	Not Used											
	ST23	Not Used											
	IFPF2	Interface Color Pixel Format		"011"=12-bit/pixel									
	IFPF1	Definition		"101"=16-bit/pixel									
	IFPF0			"110"=18-bit/pixel									
	IDMON	Idle Mode On/Off		"1"=On,"0"=Off									

	PTLON	Partial Mode On/Off	“1”=On, “0”=Off																									
	SLOUT	Sleep In/Out	“1”=On, “0”=Off																									
	NORON	Display Normal Mode On/Off	“1”=Normal Display, “0”=Normal Display Off																									
	VSSON	Vertical Scrolling Status	“1”=Scroll on, “0”=Scroll off																									
	ST14	Horizontal Scroll Status	“0”																									
	INVON	Inversion Status	“1”=On, “0”=Off																									
	ST12	All Pixels On(Not Used)	“0”																									
	ST11	All Pixels On(Not Used)	“0”																									
	DISON	Display On/Off	“1”=On, “0”=Off																									
	TEON	Tearing effect line on/off	“1”=On, “0”=Off																									
	GCS2	Gamma Curve Selection	“000”=GC0 “001”=GC1 “010”=GC2 “011”=GC3 “100” to “111” = Not defined																									
	GCS1																											
	GCS																											
	TELOM	Tearing effect line mode	“0”=mode1, “1”=mode2																									
	STO	For Future Use	“0”																									
Note: For Bits ST30 to ST28, also refer to Section 8-11																												
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>				Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
Status	Availability																											
Normal Mode On, Idle Mode Off, Sleep Out	Yes																											
Normal Mode On, Idle Mode On, Sleep Out	Yes																											
Partial Mode On, Idle Mode Off, Sleep Out	Yes																											
Partial Mode On, Idle Mode On, Sleep Out	Yes																											
Sleep In	Yes																											
Default	<table><tr><th rowspan="2">Status</th><th colspan="4">Default Value(ST31 to ST0)</th></tr><tr><th>ST[31-24]</th><th>ST[23-16]</th><th>ST[15-8]</th><th>ST[7-0]</th></tr><tr><td>Power On Sequence</td><td>0000-0000</td><td>0110-0001</td><td>0000-0000</td><td>0000-0000</td></tr><tr><td>SW Reset</td><td>0xxx-xxx0</td><td>0xxx-0001</td><td>0000-0000</td><td>0000-0000</td></tr><tr><td>HW Reset</td><td>0000-0000</td><td>0110-0001</td><td>0000-0000</td><td>0000-0000</td></tr></table>				Status	Default Value(ST31 to ST0)				ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]	Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000	SW Reset	0xxx-xxx0	0xxx-0001	0000-0000	0000-0000	HW Reset	0000-0000	0110-0001	0000-0000	0000-0000
Status	Default Value(ST31 to ST0)																											
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]																								
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000																								
SW Reset	0xxx-xxx0	0xxx-0001	0000-0000	0000-0000																								
HW Reset	0000-0000	0110-0001	0000-0000	0000-0000																								



### 14.2.5 Read Display Power Mode (0Ah)

0AH		RDDPM (Read Display Power Mode)																							
Inst / Para	D/C X	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	0	0	1	0	1	0	0Ah												
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	X												
2 <sup>nd</sup> Parameter	1		1	x	D7	D6	D5	D4	D3	D2	D1	D0	08h												
Description	This command indicates the current status of the display as described in the table below:																								
	Bit	Description					Value																		
	D7	Booster Voltage Status					“1”=Booster on, “0”=Booster off																		
	D6	Idle Mode On/Off					“1”=Idle Mode On, “0”=Idle Mode Off																		
	D5	Partial Mode On/Off					“1”=Partial Mode on, “0”=Partial Mode Off																		
	D4	Sleep In/Out					“1”=Sleep Out, “0”=Sleep In																		
	D3	Display Normal Mode On/Off					“1”=Normal Display, “0”=Partial Display																		
	D2	Display On/Off					“1”=Display On, “0”=Display Off																		
	D1	Not Defined					Set to ‘0’																		
D0	Not Defined					Set to ‘0’																			
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>0000_1000(08h)</td></tr><tr><td>SW Reset</td><td>0000_1000(08h)</td></tr><tr><td>HW Reset</td><td>0000_1000(08h)</td></tr></table>													Status	Default Value(D7 to D0)	Power On Sequence	0000_1000(08h)	SW Reset	0000_1000(08h)	HW Reset	0000_1000(08h)				
	Status	Default Value(D7 to D0)																							
	Power On Sequence	0000_1000(08h)																							
	SW Reset	0000_1000(08h)																							
HW Reset	0000_1000(08h)																								
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDPM(0Ah)</div><div>Send D[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDPM(0Ah)</div><div>Dummy Read</div><div>Send D [7:0]</div></div></div><div><div>Host</div><div>Driver</div></div></div>																								
	<div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

### 14.2.6 Read Display MADCTL (0Bh)

0BH	RDDMADCTL (Read Display MADCTL)																								
	D/CX	RDX	WRX	D17-0	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	0	0	1	0	1	1	0Bh												
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x												
2 <sup>nd</sup> Parameter	1		1	x	D7	D6	D5	D4	D3	D2	D1	D0	00h												
Description	This command indicates the current status of the display as described in the table below:																								
	Bit	Description						Value																	
	D7	Page Address Order						“1”=Decrement, “0”=Increment																	
	D6	Column Address Order						“1”=Decrement, “0”=Increment																	
	D5	Page/Column Order						“1”=Row/column exchange(MV=1) “0”=Normal(MV=0)																	
	D4	Line Address Order						“1”=LCD Refresh Bottom to Top “0”=LCD Refresh Top to Bottom																	
	D3	RGB/BGR Order						“1”=BGR, “0”=RGB																	
	D2	Display Data Latch Order						“1”=LCD Refresh right to left “0”=LCD Refresh left to right																	
	D1	Switching between Segment outputs and RAM						Set to ‘0’																	
D0	Switching between Common outputs and RAM						Set to ‘0’																		
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>0000_0000(00h)</td></tr><tr><td>SW Reset</td><td>No Change</td></tr></table>													Status	Default Value(D7 to D0)	Power On Sequence	0000_0000(00h)	SW Reset	No Change						
Status	Default Value(D7 to D0)																								
Power On Sequence	0000_0000(00h)																								
SW Reset	No Change																								
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDMADCTR(0Bh)</div><div>↓</div><div>Send D[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDMADCTR(0Bh)</div><div>↓</div><div>Dummy Read</div><div>↓</div><div>Send D [7:0]</div></div></div><div><div>Host</div><div>Driver</div></div></div> <div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

### 14.2.7 Read Display Pixel Format (0Ch)

0CH		RDDCOLMOD (Read Display COLMOD)											
	D/C X	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	0	0	1	1	0	0	0Ch
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x
2 <sup>nd</sup> Parameter	1		1	x	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h
Description	This command indicates the current status of the display as described in the table below:												
	Bit		Description					Value					
	D7	VIPF3	RGB Interface Color Format					0101 = 16 bit/pixel (1 time data transfer)					
	D6	VIPF2						0110 = 18 bit/pixel (1 time data transfer)					
	D5	VIPF1						1110 = 18 bit/pixel (3 times data transfer)					
	D4	VIPF0						The other = not defined					
	D3	D3						"0" (Not used)					
	D2	IFPF2	Control Interface Color Format					"011"=12 bit/pixel					
	D1	IFPF 1						"101"=16 bit/pixel					
	D0	IFPF 0						"110"=18 bit/pixel					
		The others = not defined											
Register Availability													
Default													
Flow Chart													

## 14.2.8 Read Display Image Mode (0Dh)

0DH	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	0	0	1	1	0	1	0Dh
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x
2 <sup>nd</sup> Parameter	1		1	x	D7	D6	D5	D4	D3	D2	D1	D0	00h
Description													
	Bit	Description					Value						
	D7	Vertical Scrolling On/Off					“1”=Vertical scrolling is On, “0”=Vertical scrolling is Off						
	D6	Horizontal Scrolling On/Off					“0”(Not used)						
	D5	Inversion On/Off					“1”=Inversion is On, “0”=Inversion is Off						
	D4	All Pixels On					“0” (Not used)						
	D3	All Pixel Off					“0” (Not used)						
	D2	Gamma Curve Selection					“000”=GC0; “001”=GC1; “010”=GC2; “011”=GC3 “100” to “111” = Not defined						
	D1												
	D0												
Register Availability													
	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
	Sleep In								Yes				
Default													
	Status					Default Value(D7 to D0)							
	Power On Sequence					0000_0000(00h)							
SW Reset					0000_0000(00h)								

### 14.2.9 Read Display Signal Mode (0Eh)

0EH	RDDSM (Read Display Signal Mode)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	0	0	1	1	1	0	0Eh												
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x												
2 <sup>nd</sup> Parameter	1		1	x	D7	D6	D5	D4	D3	D2	D1	D0	00h												
Description	This command indicates the current status of the display as described in the table below:																								
	Bit	Description					Value																		
	D7	Tearing Effect Line On/Off					“1”=On, “0”=Off																		
	D6	Tearing Effect Line Mode					“0”=mode1, “1”=mode2																		
	D5	Horizontal Sync. (RGB I/F) On / Off					“1”=On, “0”=Off																		
	D4	Vertical Sync. (RGB I/F) On / Off					“1”=On, “0”=Off																		
	D3	Pixel Clock (PCLK, RGB I/F) On / Off					“1”=On, “0”=Off																		
	D2	Data Enable (DE , RGB I/F) On / Off					“1”=On, “0”=Off																		
	D1	Not Used																							
	D0	Not Used																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>0000_0000(00h)</td></tr><tr><td>SW Reset</td><td>0000_0000(00h)</td></tr></table>													Status	Default Value(D7 to D0)	Power On Sequence	0000_0000(00h)	SW Reset	0000_0000(00h)						
	Status	Default Value(D7 to D0)																							
	Power On Sequence	0000_0000(00h)																							
SW Reset	0000_0000(00h)																								
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDID(0Eh)</div><div>↓</div><div>Send D[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDPM(0Eh)</div><div>↓</div><div>Dummy Read</div><div>↓</div><div>Send D [7:0]</div></div></div><div><div>Host</div><div>Driver</div></div></div> <div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

### 14.2.10 Read Display Signal Mode (0Fh)

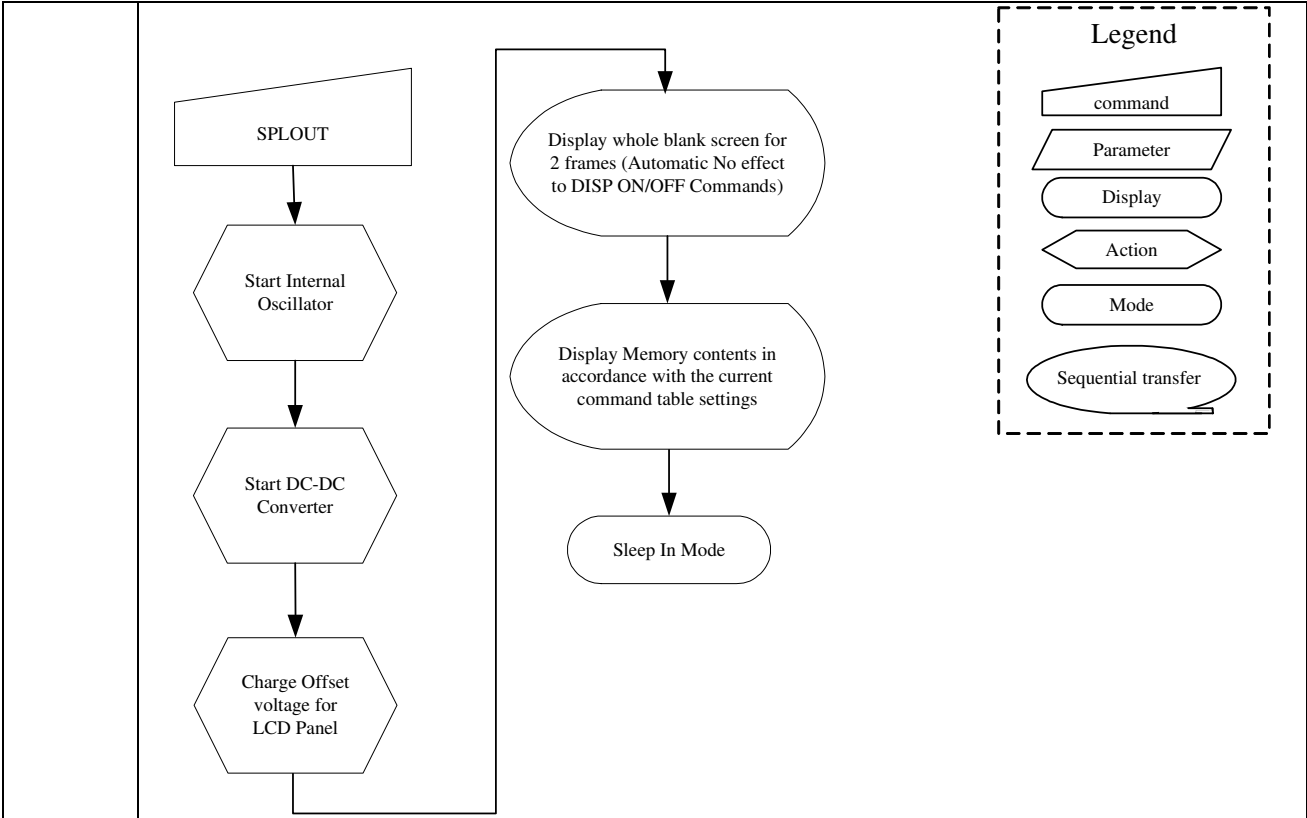
0EH		RDDSM (Read Display Signal Mode)																							
	D/C X	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	0	0	1	1	1	1	0Fh												
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x												
2 <sup>nd</sup> Parameter	1		1	x	D7	D6	D5	D4	D3	D2	D1	D0	00h												
Description	This command indicates the current status of the display as described in the table below:																								
	Bit	Description					Value																		
	D7	Register Loading Detection																							
	D6	Functionality Detection																							
	D5	Not Used					“0”																		
	D4	Not Used					“0”																		
	D3	Not Used					“0”																		
	D2	Not Used					“0”																		
	D1	Not Used					“0”																		
	D0	Not Used					“0”																		
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
	Sleep In	Yes																							
Default	<table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>0000_0000(00h)</td></tr><tr><td>SW Reset</td><td>0000_0000(00h)</td></tr></table>													Status	Default Value(D7 to D0)	Power On Sequence	0000_0000(00h)	SW Reset	0000_0000(00h)						
	Status	Default Value(D7 to D0)																							
	Power On Sequence	0000_0000(00h)																							
	SW Reset	0000_0000(00h)																							
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDID(0Fh)</div><div>↓</div><div>Send 2nd Parameter</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDPM(0Fh)</div><div>↓</div><div>Dummy Read</div><div>↓</div><div>Send 2nd Parameter</div></div></div><div><div>Host</div><div>Driver</div></div></div>																								
	<div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

### 14.2.11 Sleep In (10h)

10H	SLPIN (Sleep In)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	0	1	0	0	0	0	10h												
Parameter	No Parameter																								
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. MCU interface and memory are still working and the memory keeps its contents.																								
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode						
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
SW Reset	Sleep In Mode																								
Flow Chart	<div>It takes 120msec to get into Sleep In mode after SLPIN command issued.</div> <div><pre>graph TD     SLPIN[/SLPIN/] --&gt; Display([Display whole blank screen (automatic No effect to DISP ON/OFF command)])     Display --&gt; Drain{{Drain charge from LCD panel}}     Drain --&gt; StopDCDC{{Stop DC/DC Converter}}     StopDCDC --&gt; StopOscillator{{Stop Internal Oscillator}}     StopOscillator --&gt; SleepIn([Sleep In Mode])</pre><div><b>Legend</b> command: trapezoid Parameter: parallelogram Display: rounded rectangle Action: hexagon Mode: oval Sequential transfer: oval with a loop</div></div>																								

## 14.2.12 Sleep Out (11h)

11H	SLPOUT (Sleep Out)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	0	1	0	0	0	1	11h												
Parameter	No Parameter																								
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.																								
Restriction	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).</p> <p>It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.</p> <p>The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p> <p>This command has no effect when module is already in sleep out mode.</p> <p>Sleep Out Mode can only be left by HW Reset, Software Reset (01h), Sleep In (10h), or a NMI event trigger.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr><tr><td>HW Reset</td><td>Sleep In Mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
SW Reset	Sleep In Mode																								
HW Reset	Sleep In Mode																								
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued.																								



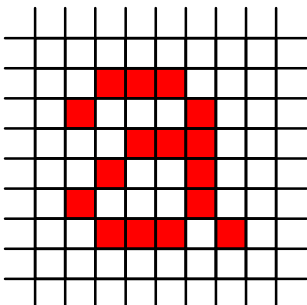
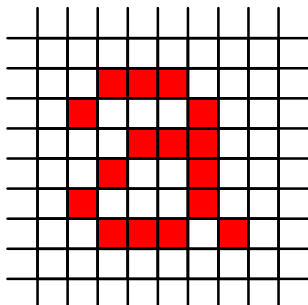
### 14.2.13 Partial Mode On (12h)

12H	PTLON (Partial Mode On)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	0	1	0	0	1	0	12h												
Parameter	No Parameter																								
Description	<p>This command turns on partial mode. The partial mode is described by the Partial Area command (30h).</p> <p>To leave Partial mode, the Normal Display On command (13h) should be written.</p> <p>X = Don't care</p> <p>Note: If a command is written in a frame cycle, the command becomes effective from the next frame.</p>																								
Restriction	This command has no effect during Partial mode is active.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table>													Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On				
Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	See Partial Area (30h)																								

## 14.2.14 Normal Display Mode On (13h)

13H	PTLON (Partial Mode On)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	0	1	0	0	1	1	13h												
Parameter	No Parameter																								
Description	<p>This command returns the display to normal mode.</p> <p>Normal display mode on means Partial mode off and Scroll mode Off.</p> <p>Exit from NORON by the Partial mode On command(12h)</p> <p>X = Don't care</p> <p>Note: If a command is written in a frame cycle, the command becomes effective from the next frame.</p>																								
Restriction	This command has no effect when Normal Display mode is active.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table>													Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On				
Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.																								

### 14.2.15 Display Inversion Off (20h)

20H				PTLON (Partial Mode On)																					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	1	0	0	0	0	0	20h												
Parameter	No Parameter																								
Description	<div><div><p>This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status.</p><div><div><div>Memory</div><div></div></div><div><div>Display Panel</div><div></div></div></div><div><div></div><div></div></div><p>X = don't care</p></div></div>																								
Restriction	This command has no effect when module is already in inversion off mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode Off</td></tr><tr><td>SW Reset</td><td>Normal Display Mode Off</td></tr><tr><td>HW Reset</td><td>Normal Display Mode Off</td></tr></table>													Status	Default Value	Power On Sequence	Normal Display Mode Off	SW Reset	Normal Display Mode Off	HW Reset	Normal Display Mode Off				
Status	Default Value																								
Power On Sequence	Normal Display Mode Off																								
SW Reset	Normal Display Mode Off																								
HW Reset	Normal Display Mode Off																								
Flow Chart	<div><div><div>Display Inversion On Mode</div><div></div><div>INVOFF(20h)</div><div></div><div>Display Inversion Off Mode</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

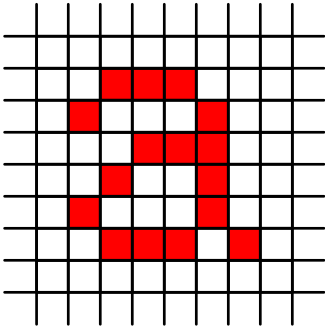
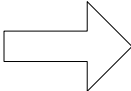
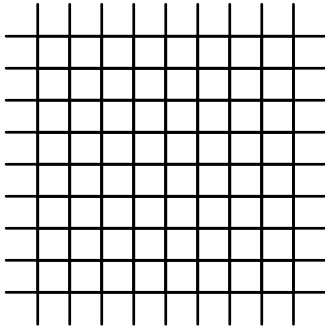
## 14.2.16 Display Inversion On (21h)

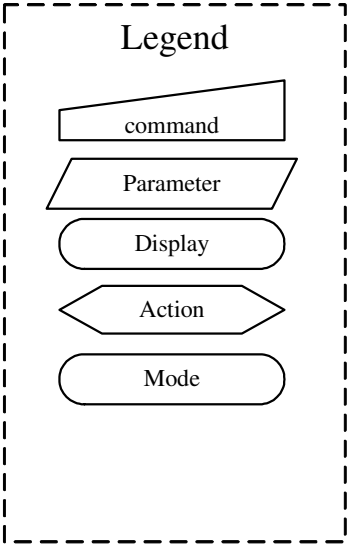
21H	PTLON (Partial Mode On)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	1	0	0	0	0	1	21h												
Parameter	No Parameter																								
Description	<p>This command is used to enter into display inversion mode.</p> <p>This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.</p> <p>This command does not change any other status.</p> <p>To exit from Display inversion On, the Display Inversion Off command(20h) should be written.</p> <div><div>Memory</div><div><div>→</div><div>Display Panel</div><div><div>X = don't care</div></div></div></div>																								
Restriction	This command has no effect when module is already in inversion on mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode Off</td></tr><tr><td>SW Reset</td><td>Normal Display Mode Off</td></tr><tr><td>HW Reset</td><td>Normal Display Mode Off</td></tr></table>													Status	Default Value	Power On Sequence	Normal Display Mode Off	SW Reset	Normal Display Mode Off	HW Reset	Normal Display Mode Off				
Status	Default Value																								
Power On Sequence	Normal Display Mode Off																								
SW Reset	Normal Display Mode Off																								
HW Reset	Normal Display Mode Off																								
Flow Chart	<div><div><div>Display Inversion On Mode</div><div>↓</div><div>INVON(21h)</div><div>↓</div><div>Display Inversion Off Mode</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

### 14.2.17 Gamma Set (26h)

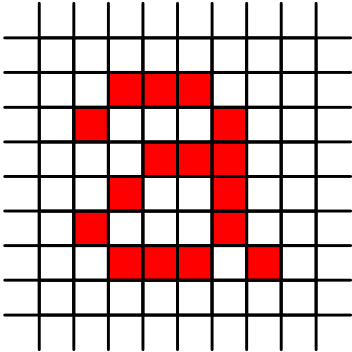
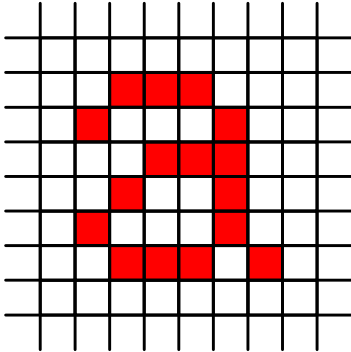
26H	GAMSET (Gamma Set)																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1		x	0	0	1	0	0	1	1	0	26h															
Parameter	1	1		x	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h															
Description	<p>This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined Gamma Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the table:</p> <table><tr><th>GC[7..0]</th><th>Parameter</th><th>Curve Selected</th></tr><tr><td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr><tr><td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr><tr><td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr><tr><td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr></table> <p>Note: All other values are undefined. X = don't care</p>													GC[7..0]	Parameter	Curve Selected	01h	GC0	Gamma Curve 1	02h	GC1	Gamma Curve 2	04h	GC2	Gamma Curve 3	08h	GC3	Gamma Curve 4
GC[7..0]	Parameter	Curve Selected																										
01h	GC0	Gamma Curve 1																										
02h	GC1	Gamma Curve 2																										
04h	GC2	Gamma Curve 3																										
08h	GC3	Gamma Curve 4																										
Restriction	Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.																											
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability																											
Normal Mode On, Idle Mode Off, Sleep Out	Yes																											
Normal Mode On, Idle Mode On, Sleep Out	Yes																											
Partial Mode On, Idle Mode Off, Sleep Out	Yes																											
Partial Mode On, Idle Mode On, Sleep Out	Yes																											
Sleep In	Yes																											
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>01h</td></tr><tr><td>SW Reset</td><td>01h</td></tr><tr><td>HW Reset</td><td>01h</td></tr></table>													Status	Default Value	Power On Sequence	01h	SW Reset	01h	HW Reset	01h							
Status	Default Value																											
Power On Sequence	01h																											
SW Reset	01h																											
HW Reset	01h																											
Flow Chart	<div><div><p>Partial Mode</p><pre>graph TD; A[GAMSET (26h)] --&gt; B[/1st Parameter: GC[7:0]/]; B --&gt; C{{New Gamma Curve Loaded}};</pre></div><div><p>Legend</p><ul style="list-style-type: none"><li>command</li><li>Parameter</li><li>Display</li><li>Action</li><li>Mode</li><li>Sequential transfer</li></ul></div></div>																											

## 14.2.18 Display Off (28h)

28H	DISPOFF (Display Off)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	1	0	1	0	0	0	28h												
Parameter	No Parameter																								
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.																								
	This command makes no change of contents of frame memory.																								
	This command does not change any other status.																								
	There will be no abnormal visible effect on the display.																								
	Exit from this command by Display On(29h)																								
Description	<div><div><div>Memory</div></div><div></div><div><div>Display Panel</div></div></div>																								
	X = don't care																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>SW Reset</td><td>Display Off</td></tr><tr><td>HW Reset</td><td>Display Off</td></tr></table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
SW Reset	Display Off																								
HW Reset	Display Off																								
Flow Chart																									

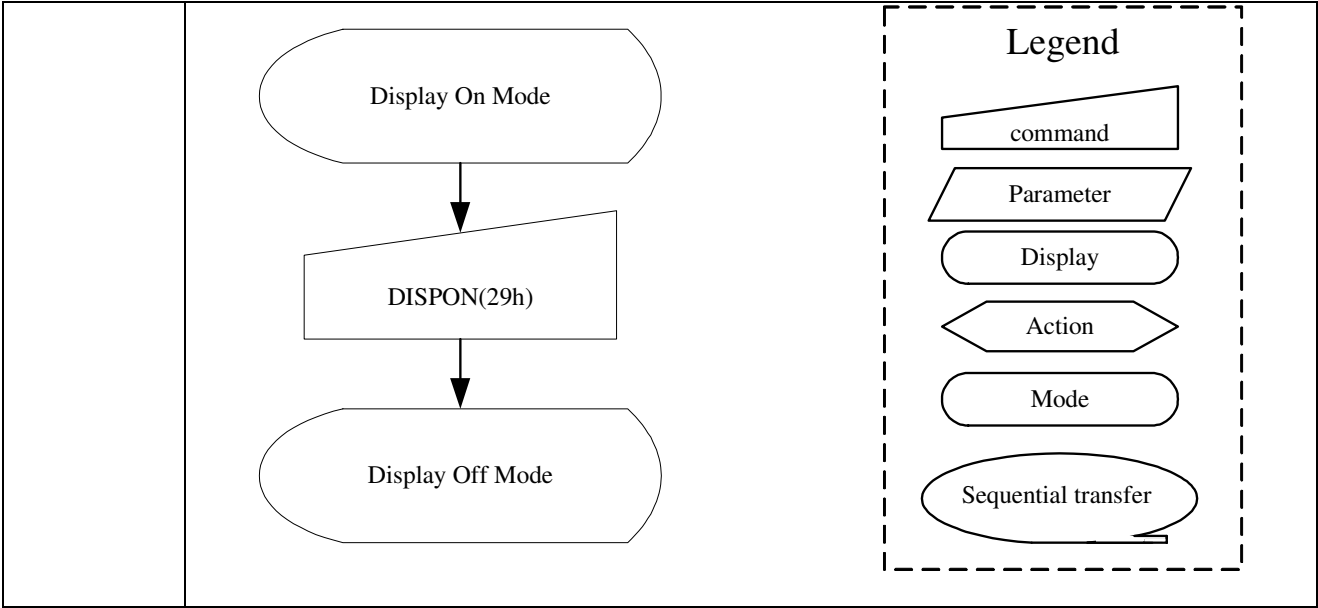


14.2.19 Display On (29h)

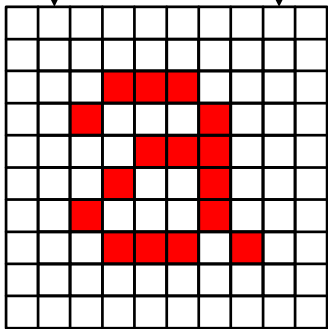
29H	DISPON (Display On)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter												
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p>												
	<div><div>Memory</div><div>Display Panel</div></div> <p>X = don't care</p>												
Restriction	This command has no effect when module is already in display on mode.												

Register  
Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	

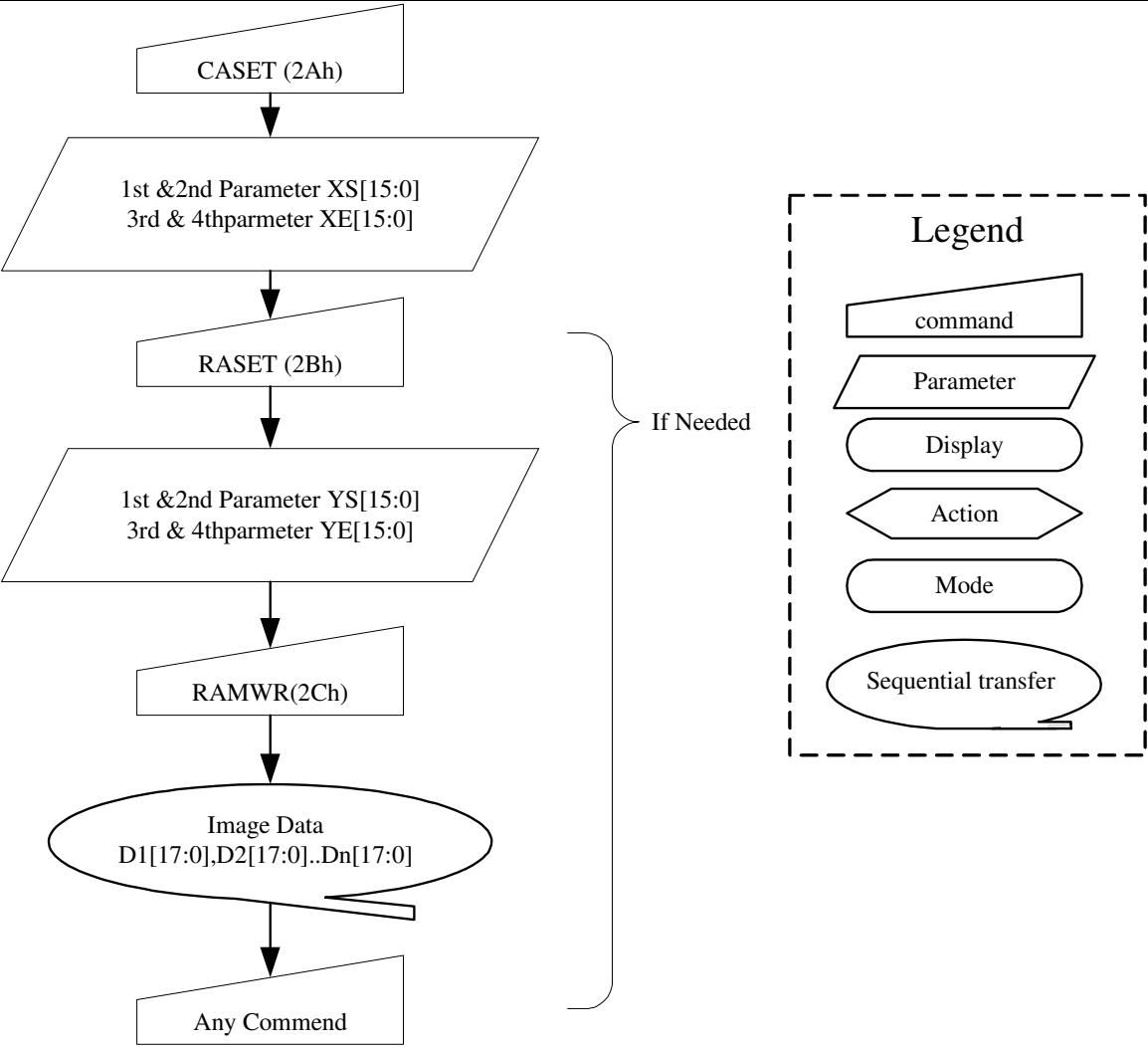


## 14.2.20 Column Address Set (2Ah)

2AH	CASET (Column Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	1	0	1	0	1	0	2Ah
1 <sup>st</sup> Parameter	1	1		x	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-
2 <sup>nd</sup> Parameter	1	1		x	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-
3 <sup>rd</sup> Parameter	1	1		x	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-
4 <sup>th</sup> Parameter	1	1		x	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of XS[15:0] and XE[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.</p> <div style="text-align: center;">  </div> <p>X = don't care</p>												
Restriction	<p>XS [15:0] always must be equal to or less than XE[15:0].</p> <p>When XS[15:0] or XE[15:0] is greater than maximum address like below, data of out of range will be ignored.</p> <ol style="list-style-type: none"> <li>132X132 memory base (GM='101') (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 131(0083h)</math>:MV="0") (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 131(0083h)</math>:MV="1")</li> <li>130X130 memory base (GM='100') (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 129(0081h)</math>:MV="0") (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 129(0081h)</math>:MV="1")</li> <li>128X160 memory base (GM='011') (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 127(007Fh)</math>:MV="0") (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 159(009Fh)</math>:MV="1")</li> <li>120X160 memory base (GM='010') (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 119(0077h)</math>:MV="0") (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 159(009Fh)</math>:MV="1")</li> <li>128X128 memory base (GM='001') (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 127(007Fh)</math>:MV="0") (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 127(007Fh)</math>:MV="1")</li> <li>132X162 memory base (GM='000') (Parameter range: <math>0 \leq XS[15:0] \leq XE[15:0] \leq 131(0083h)</math>:MV="0")</li> </ol>												

	(Parameter range: 0 ≤ XS[15:0] ≤ XE[15:0] ≤ 127(00A1h):MV="1")																					
	X = Don't care																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
	Status	Availability																				
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																				
	Normal Mode On, Idle Mode On, Sleep Out	Yes																				
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																				
	Partial Mode On, Idle Mode On, Sleep Out	Yes																				
Sleep In	Yes																					
Default	1. 132 x 132 memory base(GM='101')																					
	<table><tr><th>Status</th><th colspan="3">Default Value</th></tr><tr><td>XS[15:0]</td><td>XE[15:0]</td><td>EX[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">0083h(131)</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>0083h(131)</td><td>0083h(131)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">0083h(131)</td></tr></table>	Status	Default Value			XS[15:0]	XE[15:0]	EX[15:0] (MV=1)	Power On Sequence	0000h	0083h(131)		S/W Reset	0000h	0083h(131)	0083h(131)	HW Reset	0000h	0083h(131)			
		Status	Default Value																			
		XS[15:0]	XE[15:0]	EX[15:0] (MV=1)																		
		Power On Sequence	0000h	0083h(131)																		
		S/W Reset	0000h	0083h(131)	0083h(131)																	
	HW Reset	0000h	0083h(131)																			
	2. 130 x 130 memory base(GM='100')																					
	<table><tr><th>Status</th><th colspan="3">Default Value</th></tr><tr><td>XS[15:0]</td><td>XE[15:0]</td><td>EX[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">0081h(129)</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>0081h(129)</td><td>0081h(129)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">0081h(129)</td></tr></table>	Status	Default Value			XS[15:0]	XE[15:0]	EX[15:0] (MV=1)	Power On Sequence	0000h	0081h(129)		S/W Reset	0000h	0081h(129)	0081h(129)	HW Reset	0000h	0081h(129)			
		Status	Default Value																			
		XS[15:0]	XE[15:0]	EX[15:0] (MV=1)																		
		Power On Sequence	0000h	0081h(129)																		
		S/W Reset	0000h	0081h(129)	0081h(129)																	
	HW Reset	0000h	0081h(129)																			
	3. 128 x 160 memory base(GM='011')																					
	<table><tr><th>Status</th><th colspan="3">Default Value</th></tr><tr><td>XS[15:0]</td><td>XE[15:0]</td><td>EX[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">007Fh(127)</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>007Fh(127)</td><td>009Fh(159)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">007Fh(127)</td></tr></table>	Status	Default Value			XS[15:0]	XE[15:0]	EX[15:0] (MV=1)	Power On Sequence	0000h	007Fh(127)		S/W Reset	0000h	007Fh(127)	009Fh(159)	HW Reset	0000h	007Fh(127)			
		Status	Default Value																			
		XS[15:0]	XE[15:0]	EX[15:0] (MV=1)																		
		Power On Sequence	0000h	007Fh(127)																		
		S/W Reset	0000h	007Fh(127)	009Fh(159)																	
	HW Reset	0000h	007Fh(127)																			
	4. 120 x 160 memory base(GM='010')																					
	<table><tr><th>Status</th><th colspan="3">Default Value</th></tr><tr><td>XS[15:0]</td><td>XE[15:0]</td><td>EX[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">0077h(119)</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>007Fh(119)</td><td>009Fh(159)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">0077h(119)</td></tr></table>	Status	Default Value			XS[15:0]	XE[15:0]	EX[15:0] (MV=1)	Power On Sequence	0000h	0077h(119)		S/W Reset	0000h	007Fh(119)	009Fh(159)	HW Reset	0000h	0077h(119)			
		Status	Default Value																			
		XS[15:0]	XE[15:0]	EX[15:0] (MV=1)																		
		Power On Sequence	0000h	0077h(119)																		
		S/W Reset	0000h	007Fh(119)	009Fh(159)																	
	HW Reset	0000h	0077h(119)																			
	5. 128 x 128 memory base(GM='001')																					
	<table><tr><th>Status</th><th colspan="3">Default Value</th></tr><tr><td>XS[15:0]</td><td>XE[15:0]</td><td>EX[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">007Fh(127)</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>007Fh(127)</td><td>009Fh(127)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">0077h(119)</td></tr></table>	Status	Default Value			XS[15:0]	XE[15:0]	EX[15:0] (MV=1)	Power On Sequence	0000h	007Fh(127)		S/W Reset	0000h	007Fh(127)	009Fh(127)	HW Reset	0000h	0077h(119)			
		Status	Default Value																			
		XS[15:0]	XE[15:0]	EX[15:0] (MV=1)																		
		Power On Sequence	0000h	007Fh(127)																		
		S/W Reset	0000h	007Fh(127)	009Fh(127)																	
	HW Reset	0000h	0077h(119)																			
	6. 132 x 162 memory base(GM='000')																					
<table><tr><th>Status</th><th colspan="3">Default Value</th></tr><tr><td>XS[15:0]</td><td>XE[15:0]</td><td>EX[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">0083h(131)</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>0083h(131)</td><td>00A1h(161)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">0083h(131)</td></tr></table>	Status	Default Value			XS[15:0]	XE[15:0]	EX[15:0] (MV=1)	Power On Sequence	0000h	0083h(131)		S/W Reset	0000h	0083h(131)	00A1h(161)	HW Reset	0000h	0083h(131)				
	Status	Default Value																				
	XS[15:0]	XE[15:0]	EX[15:0] (MV=1)																			
	Power On Sequence	0000h	0083h(131)																			
	S/W Reset	0000h	0083h(131)	00A1h(161)																		
HW Reset	0000h	0083h(131)																				

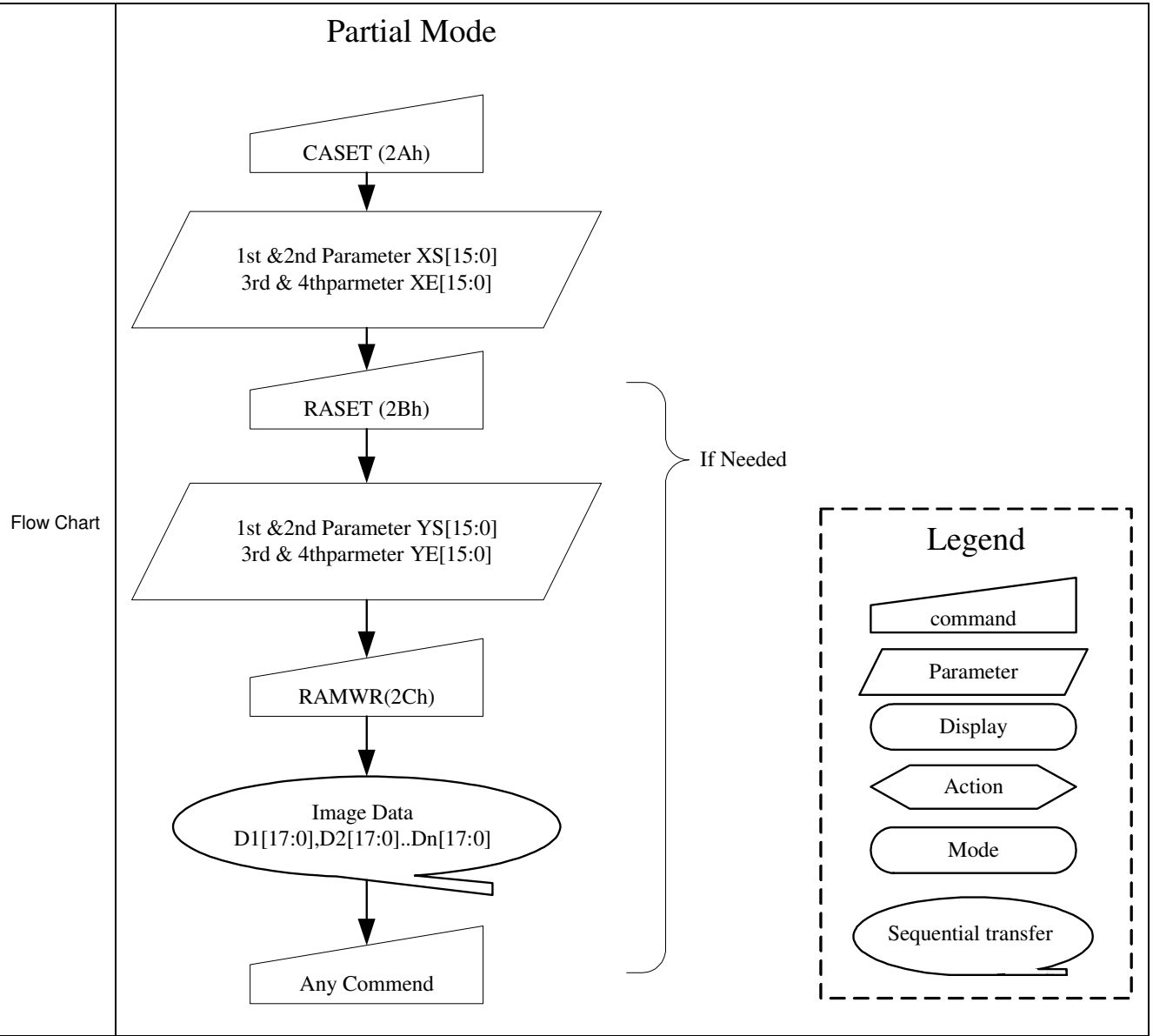
Flow Chart



## 14.2.21 Page Address Set (2Bh)

2BH	PASET (Page Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	1	0	1	0	1	1	2Bh
1 <sup>st</sup> Parameter	1	1		x	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-
2 <sup>nd</sup> Parameter	1	1		x	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-
3 <sup>rd</sup> Parameter	1	1		x	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-
4 <sup>th</sup> Parameter	1	1		x	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-
Description	<p>This command is used to define area of frame memory where MCU can access.</p> <p>This command makes no change on the other driver status.</p> <p>The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.</p> <p>Each value represents one Page line in the Frame Memory.</p> <div style="text-align: center;"> </div>												
Restriction	<p>YS [15:0] always must be equal to or less than EP [15:0].</p> <p>When YS[15:0] or YE[15:0] is greater than maximum row address like below, data of out of range will be ignored.</p> <ol style="list-style-type: none"> <li>132X132 memory base (GM='101')           <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 131(0083h)</math>):MV="0"</p> <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 131(0083h)</math>):MV="1"</p> </li> <li>130X130 memory base (GM='100')           <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 129(0081h)</math>):MV="0"</p> <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 129(0081h)</math>):MV="1"</p> </li> <li>128X160 memory base (GM='011')           <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 159(009Fh)</math>):MV="0"</p> <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 127(007Fh)</math>):MV="1"</p> </li> <li>120X160 memory base (GM='010')           <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 159(009Fh)</math>):MV="0"</p> <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 119(0077h)</math>):MV="1"</p> </li> <li>128X128 memory base (GM='001')           <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 127(007Fh)</math>):MV="0"</p> <p>(Parameter range: <math>0 \leq \text{YS}[15:0] \leq \text{YE}[15:0] \leq 127(007Fh)</math>):MV="1"</p> </li> <li>132X162 memory base (GM='000')</li> </ol>												

	<div>(Parameter range: 0 ≤ YS[15:0] ≤ YE[15:0] ≤ 161(00A1h)):MV="0"</div> <div>(Parameter range: 0 ≤ YS[15:0] ≤ YE[15:0] ≤ 131(0083h)):MV="1"</div> <div>X = Don't care</div>																																																																																																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																																																																		
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Sleep In	Yes																																																																																																																
Default	<div>1. 132 x 132 memory base(GM='101')</div> <table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><td>YS[15:0]</td><td>YE[15:0]</td><td>YX[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">0083h(131)</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>0083h(131)</td><td>0083h(131)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">0083h(131)</td></tr></table> <div>2. 130 x 130 memory base(GM='100')</div> <div>3. 128X160 memory base(GM='011')</div> <div>4. 120X160 memory base(GM='010')</div> <div>5. 120X160 memory base(GM='001')</div> <div>6. 132X162 memory base(GM='000')</div> <table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><td>YS[15:0]</td><td>YE[15:0]</td><td>YX[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">0081h(129)</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>0081h(129)</td><td>0081h(129)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">0081h(129)</td></tr></table> <table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><td>YS[15:0]</td><td>YE[15:0] (MV=0)</td><td>YE[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">009Fh(159)</td></tr><tr><td>SW Reset</td><td>0000h</td><td>009Fh(159)</td><td>007Fh(127)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">009Fh(159)</td></tr></table> <table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><td>YS[15:0]</td><td>YE[15:0] (MV=0)</td><td>YE[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">009Fh(159)</td></tr><tr><td>SW Reset</td><td>0000h</td><td>009Fh(159)</td><td>0077h(119)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">009Fh(159)</td></tr></table> <table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><td>YS[15:0]</td><td>YE[15:0] (MV=0)</td><td>YE[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">007Fh(127)</td></tr><tr><td>SW Reset</td><td>0000h</td><td>007Fh(127)</td><td>007Fh(127)</td></tr><tr><td>HW Reset</td><td>0000h</td><td colspan="2">007Fh(127)</td></tr></table> <table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><td>YS[15:0]</td><td>YE[15:0] (MV=0)</td><td>YE[15:0] (MV=1)</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td colspan="2">00A1h(161)</td></tr><tr><td>SW Reset</td><td>0000h</td><td>00A1h(161)</td><td>0083h(131)</td></tr></table>			Status	Default Value			YS[15:0]	YE[15:0]	YX[15:0] (MV=1)	Power On Sequence	0000h	0083h(131)		S/W Reset	0000h	0083h(131)	0083h(131)	HW Reset	0000h	0083h(131)		Status	Default Value			YS[15:0]	YE[15:0]	YX[15:0] (MV=1)	Power On Sequence	0000h	0081h(129)		S/W Reset	0000h	0081h(129)	0081h(129)	HW Reset	0000h	0081h(129)		Status	Default Value			YS[15:0]	YE[15:0] (MV=0)	YE[15:0] (MV=1)	Power On Sequence	0000h	009Fh(159)		SW Reset	0000h	009Fh(159)	007Fh(127)	HW Reset	0000h	009Fh(159)		Status	Default Value			YS[15:0]	YE[15:0] (MV=0)	YE[15:0] (MV=1)	Power On Sequence	0000h	009Fh(159)		SW Reset	0000h	009Fh(159)	0077h(119)	HW Reset	0000h	009Fh(159)		Status	Default Value			YS[15:0]	YE[15:0] (MV=0)	YE[15:0] (MV=1)	Power On Sequence	0000h	007Fh(127)		SW Reset	0000h	007Fh(127)	007Fh(127)	HW Reset	0000h	007Fh(127)		Status	Default Value			YS[15:0]	YE[15:0] (MV=0)	YE[15:0] (MV=1)	Power On Sequence	0000h	00A1h(161)		SW Reset	0000h	00A1h(161)	0083h(131)
Status	Default Value																																																																																																																
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SW Reset	0000h	00A1h(161)	0083h(131)																																																																																																														



## 14.2.22 Memory Write (2Ch)

2CH				RAMWR (Memory Write)									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	1	0	1	1	0	0	2Ch
1 <sup>st</sup> Parameter	1	1		D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
:	1	1		x	:	:	:	:	:	:	:	:	:
N <sup>TH</sup> Parameter	1	1		D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-
Description	This command is used to transfer data from MCU to frame memory.												
	This command makes no change to the other driver status.												
	When this command is accepted, the column register and the page register are reset to the Start Column/ Start Page positions.												
	The Start Column / Start Page positions are different in accordance with MADCTL setting.												
	Then D[17:0] is stored in frame memory and the column refister and the row register incremented.												
	Sending any other command can stop frame Write.												
	X=Don't care												
Restriction	In all color modes, there is no restriction on length of parameters.												
	1. 132X132 memory base (GM='101')												
	132X132X18-bit memory can be written by this command.												
	Memory range(0000h, 0000h) -> (0083h,083h)												
	2. 130X130 memory base (GM='100')												
	130X130X18-bit memory can be written by this command.												
	Memory range(0000h, 0000h) -> (0081h,081h)												
Register Availability	3. 128X160 memory base (GM='011')												
	128X160X18-bit memory can be written by this command.												
	Memory range(0000h, 0000h) -> (007Fh,09Fh)												
	4. 120X160 memory base (GM='010')												
	120X160X18-bit memory can be written by this command.												
	Memory range(0000h, 0000h) -> (0077h,09Fh)												
	5. 128X128 memory base (GM='001')												
120X128X18-bit memory can be written by this command.													
Memory range(0000h, 0000h) -> (007Fh,007Fh)													
6. 132X162 memory base (GM='000')													
132X162X18-bit memory can be written by this command.													
Memory range(0000h, 0000h) -> (0083h,00A1h)													
Register Availability													

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr></table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared
Status	Default Value								
Power On Sequence	Contents of memory is set randomly								
SW Reset	Contents of memory is not cleared								
HW Reset	Contents of memory is not cleared								
Flow Chart	<div><div><pre>graph TD; A[CASET (2Ah)] --&gt; B([Image Data D1[17:0],D2[17:0]..Dn[17:0]]); B --&gt; C[/Any Command/];</pre></div><div><b>Legend</b><ul style="list-style-type: none"><li>command: trapezoid</li><li>Parameter: parallelogram</li><li>Display: rounded rectangle</li><li>Action: arrowhead</li><li>Mode: rounded rectangle</li><li>Sequential transfer: oval with a tail</li></ul></div></div>								

### 14.2.23 Color Setting fro 4K, 65K and 262K (2Dh)

2DH	RAMWR (Memory Write)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	1	0	1	1	0	1	2Dh												
1 <sup>st</sup> Parameter	1	1		x	x	x	R005	R004	R003	R002	R001	R000	-												
:	1	1		x	x	x	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-												
32 <sup>nd</sup> Parameter	1	1		x	x	x	R315	R314	R313	R312	R311	R310	-												
33 <sup>rd</sup> Parameter	1	1		x	x	x	G005	G004	G003	G002	G001	G000	-												
:	1	1		x	x	x	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-												
96 <sup>th</sup> Parameter	1	1		x	x	x	G635	G634	G633	G632	G631	G630	-												
97 <sup>th</sup> Parameter	1	1		x	x	x	B005	B004	B003	B002	B001	B000													
:	1	1		x	x	x	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-												
128 <sup>th</sup> Parameter	1	1		x	x	x	B315	B314	B313	B312	B311	B310	-												
Description	<p>This command is used to define the LUT for 12bit-to-18-bit color depth conversations 128-Bytes must be written to the LUT regardless of the color mode.</p> <p>In this condition, 4K-color(4-4-4), and 65K-color(5-6-5) data input are transferred 6That-6(G)-6(B) through RGB LUT table.</p> <p>This command has no effect on other commands/parameters and Contents of frame memory.</p> <p>Visible change takes effect next time the Frame Memory is written to.</p>																								
Restriction	Do not send any command before the last data is sent or LUT is not defined correctly.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is not cleared																								
HW Reset	Contents of memory is not cleared																								
Flow Chart	<div><div>Partial Mode</div><div><div>RGBSET(2Dh)</div><div>↓</div><div><div>1st Parameter</div><div>⋮</div><div>64th Parameter</div><div>65th Parameter</div><div>⋮</div><div>128th Parameter</div></div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

## 14.2.24 Memory Read (2Eh)

2EH	RAMRD (Memory Read)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	1	0	1	1	1	0	2Eh												
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x												
2 <sup>nd</sup> Parameter	1		1	x	D17	D16	D15	D14	D13	D12	D11	D10	x												
:	1		1	x	:	:	:	:	:	:	:	:	x												
N <sup>th</sup> Parameter	1		1	x	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	x												
Description	<p>This command is used to transfer data from frame memory to MCU.</p> <p>This command makes no change to other driver status.</p> <p>When this command is accepted, the column register and then row register are reset to the Start Column/ Start Row positions.</p> <p>The Start Column / Start Row positions are different in accordance with MADCTL setting.</p> <p>Then D [17:0] is read back from the frame memory and the column register and the row register incremented.</p> <p>Frame Read can be stopped by sending any other command.</p> <p>“Display Data Format” for color coding(18 bit cases), when there is used 8,9,16 or 18 data lines for image data.</p> <p>X = Don’t care</p>																								
Restriction	<p>In all color modes, the Frame Read is always 24 bit so there is no restriction on length of parameters.</p> <p>Note: Memory Read is only possible via the Parallel Interface</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is not cleared																								
HW Reset	Contents of memory is not cleared																								
Flow Chart	<div><div><div>CASET (2Eh)</div><div>Dummy Read</div><div>Image Data D1[17:0],D2[17:0]..Dn[17:0]</div><div>Any Command</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

### 14.2.25 Partial Area (30h)

30H	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	1	1	0	0	0	0	30h
1 <sup>st</sup> Parameter	1	1		x	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-
2 <sup>nd</sup> Parameter	1	1		x	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-
3 <sup>rd</sup> Parameter	1	1		x	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-
4 <sup>th</sup> Parameter	1	1		x	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

If End Row>Start Row when MADCTL B4=0:



Description

	<div><div><div><div><div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><d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## 14.2.26 Vertical Scrolling Definition (33h)

33H	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	1	1	0	0	1	1	33h
1 <sup>st</sup> Parameter	1	1		x	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	-
2 <sup>nd</sup> Parameter	1	1		x	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	-
3 <sup>rd</sup> Parameter	1	1		x	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	-
4 <sup>th</sup> Parameter	1	1		x	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	-
5 <sup>th</sup> Parameter	1	1		x	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	-
6 <sup>th</sup> Parameter	1	1		x	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	-

This command defines the Vertical Scrolling Area of the display.

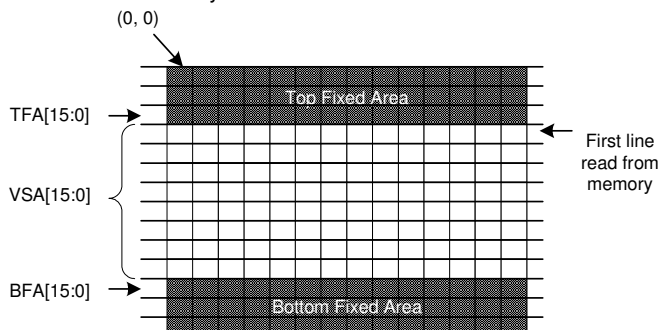
When MADCTL ML=0

Th<sup>e</sup> 1<sup>st</sup> & 2<sup>nd</sup> parameter TFA[15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

Th<sup>e</sup> 3<sup>rd</sup> & 4<sup>th</sup> parameter VSA[15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

Th<sup>e</sup> 5<sup>th</sup> & 6<sup>th</sup> parameter BFA[15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Description

When MADCTL ML=1

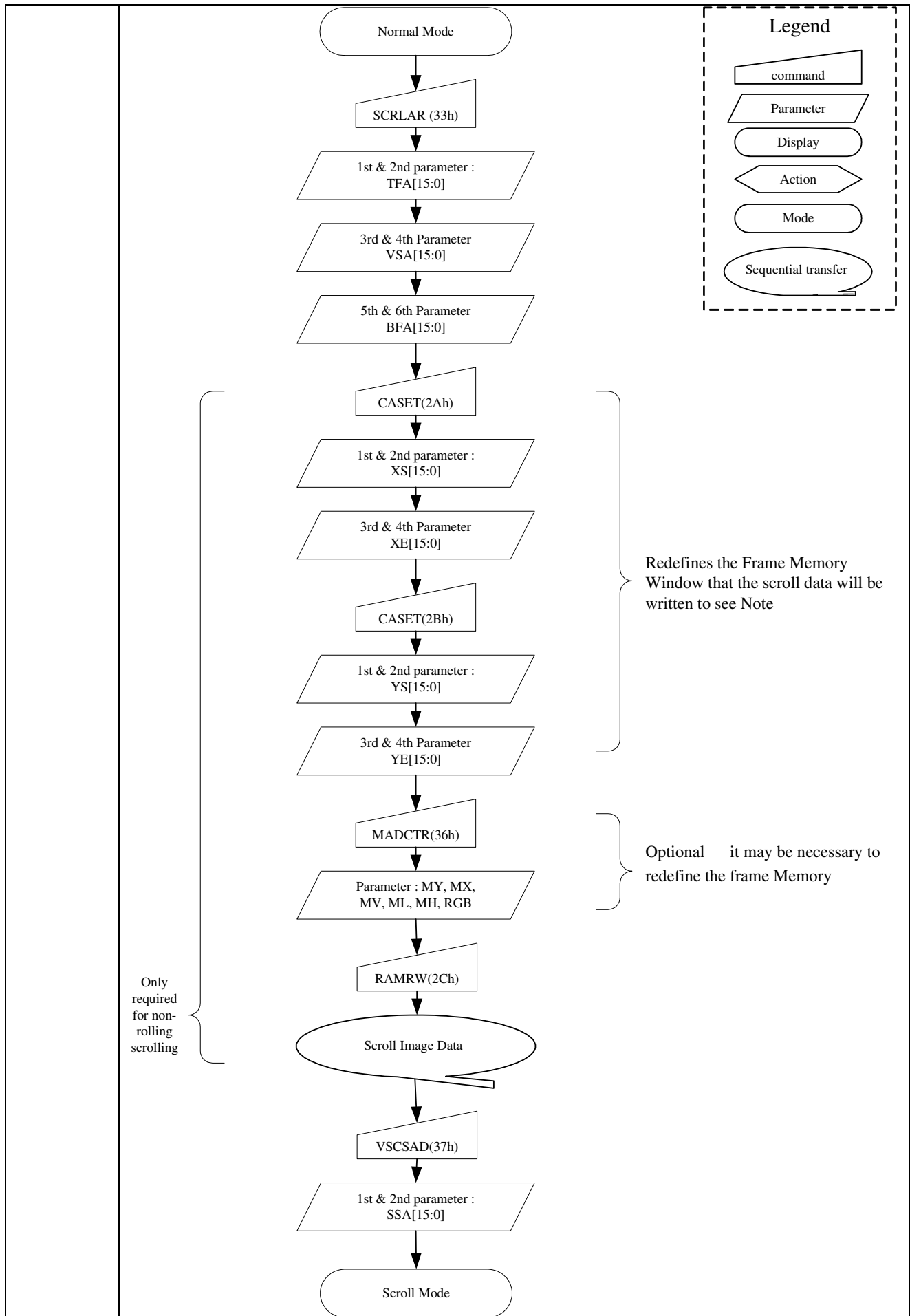
Th<sup>e</sup> 1<sup>st</sup> & 2<sup>nd</sup> parameter TFA[15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

Th<sup>e</sup> 3<sup>rd</sup> & 4<sup>th</sup> parameter VSA[15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

Th<sup>e</sup> 5<sup>th</sup> & 6<sup>th</sup> parameter BFA[15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



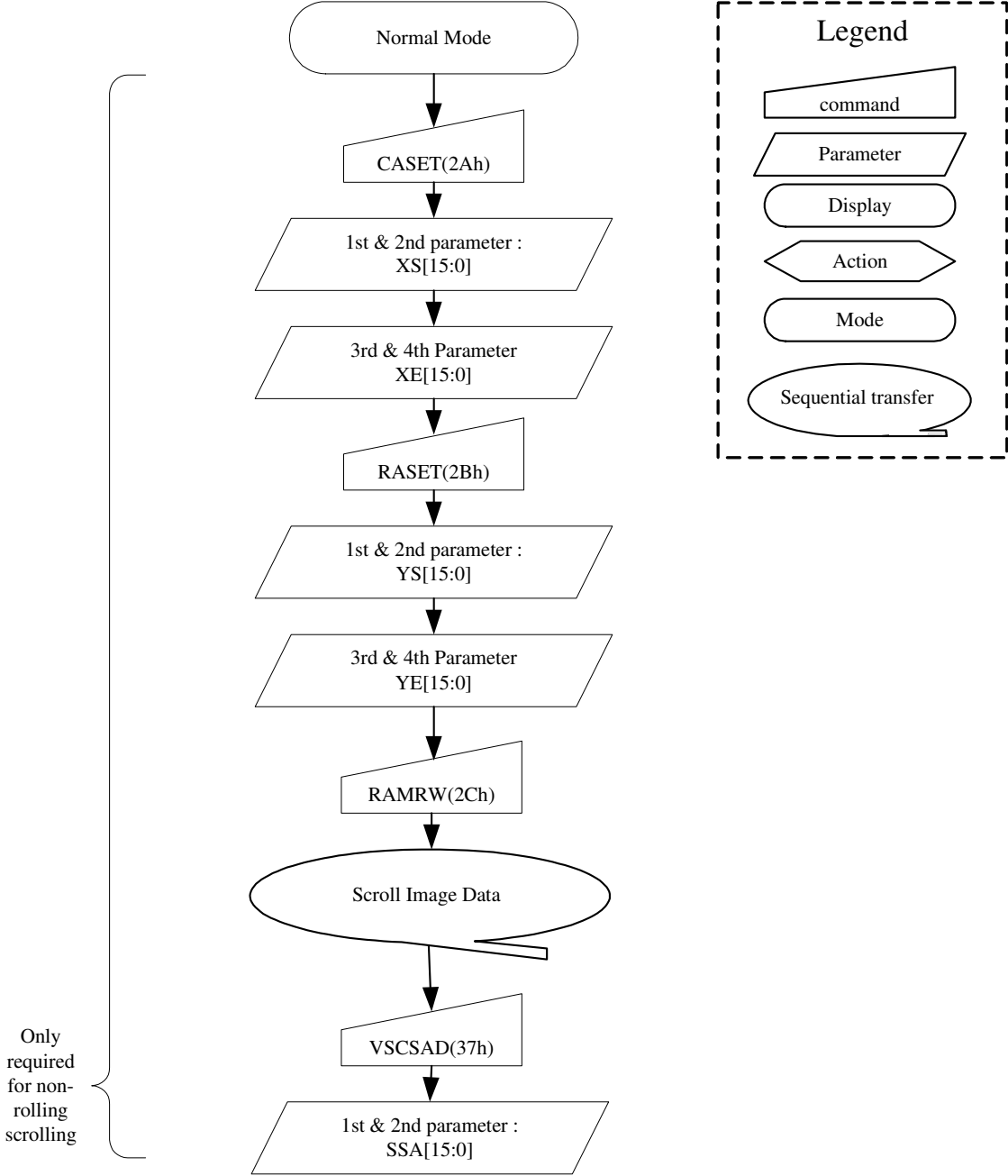
Restriction	<p>The condition is (TFA+VSA+BFA)=128 in 128RGBx128 (GM="001")</p> <p>The condition is (TFA+VSA+BFA)=130 in 130RGBx130 (GM="100")</p> <p>The condition is (TFA+VSA+BFA)=132 in 132RGBx132 (GM="101")</p> <p>The condition is (TFA+VSA+BFA)=160 in 128RGBx160 (GM="011") or 120RGBx160(GM="010")</p> <p>The condition is (TFA+VSA+BFA)=162 in 132RGBx162(GM="000")</p> <p>Otherwise Scrolling mode is undefined.</p> <p>In Vertical Scroll Mode, MADCTL parameter MV should be set to '0' – this affects the Frame memory Write.</p>																																																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																									
Status	Availability																																																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																																																					
Sleep In	Yes																																																					
Default	<table><tr><th rowspan="2">Status</th><th colspan="8">Default Value</th></tr><tr><th>TFA[15:0]</th><th colspan="6">VSA[15:0]</th><th>BFA[15:0]</th></tr><tr><td>GM</td><td>"xx"</td><td>"101"</td><td>"100"</td><td>"011"</td><td>"010"</td><td>"001"</td><td>"000"</td><td>"xx"</td></tr><tr><td>Power On Sequence</td><td>0000h</td><td>0083h</td><td>0081h</td><td>00A0h</td><td>00A0h</td><td>0080h</td><td>00A2h</td><td>0000h</td></tr><tr><td>SW Reset</td><td>0000h</td><td>0083h</td><td>0081h</td><td>00A0h</td><td>00A0h</td><td>0080h</td><td>00A2h</td><td>0000h</td></tr><tr><td>HW Reset</td><td>0000h</td><td>0083h</td><td>0081h</td><td>00A0h</td><td>00A0h</td><td>0080h</td><td>00A2h</td><td>0000h</td></tr></table>	Status	Default Value								TFA[15:0]	VSA[15:0]						BFA[15:0]	GM	"xx"	"101"	"100"	"011"	"010"	"001"	"000"	"xx"	Power On Sequence	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h	SW Reset	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h	HW Reset	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h
Status	Default Value																																																					
	TFA[15:0]	VSA[15:0]						BFA[15:0]																																														
GM	"xx"	"101"	"100"	"011"	"010"	"001"	"000"	"xx"																																														
Power On Sequence	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h																																														
SW Reset	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h																																														
HW Reset	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h																																														
Flow Chart	<p>1. To enter Vertical Scroll Mode:</p>																																																					



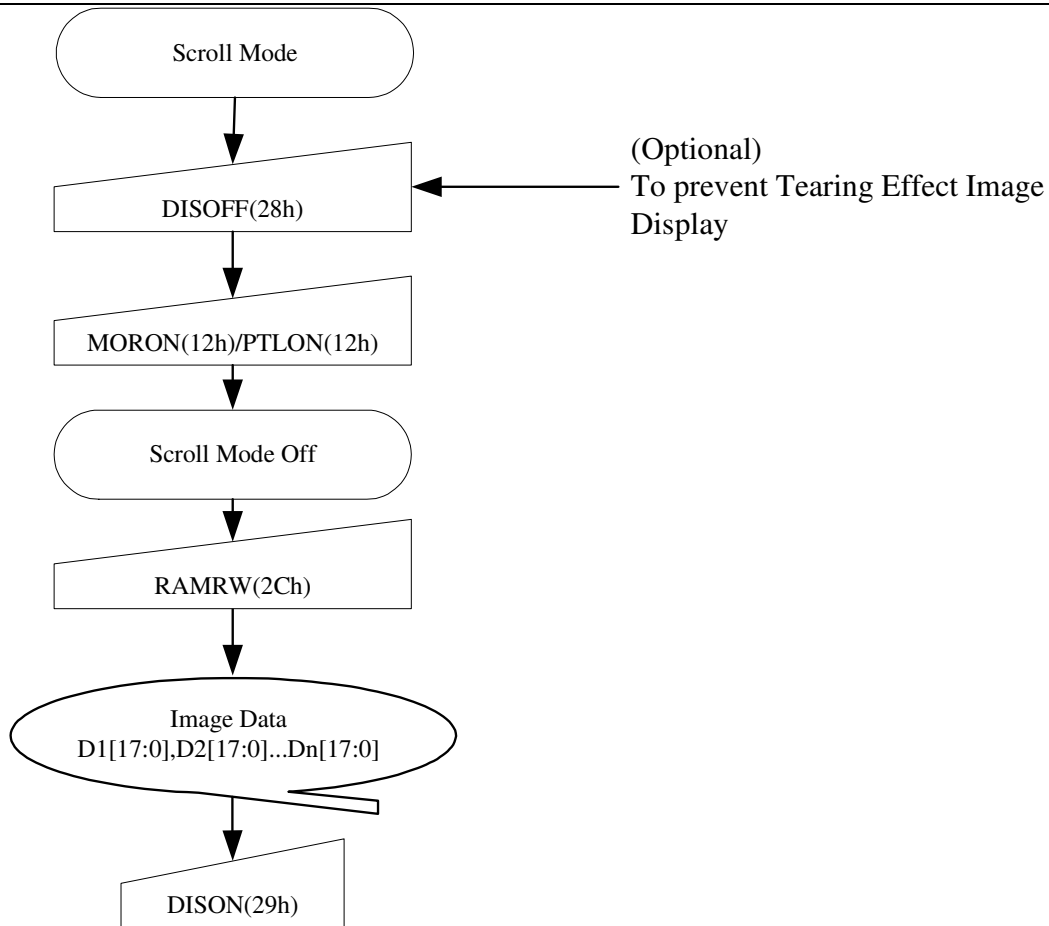
Note 1

The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:



V. . 3. To Leave Vertical Scroll Mode:

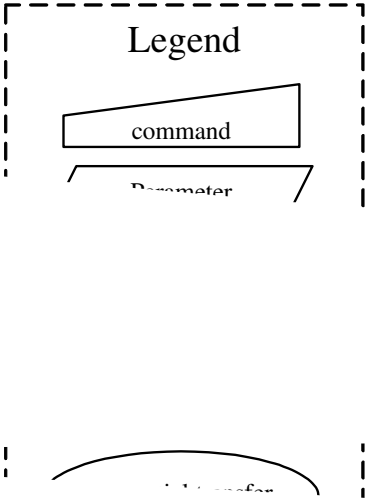
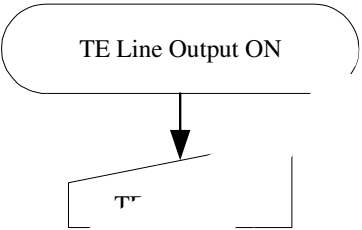


Note2: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

14.2.27 Tearing Effect Line Off (34h)

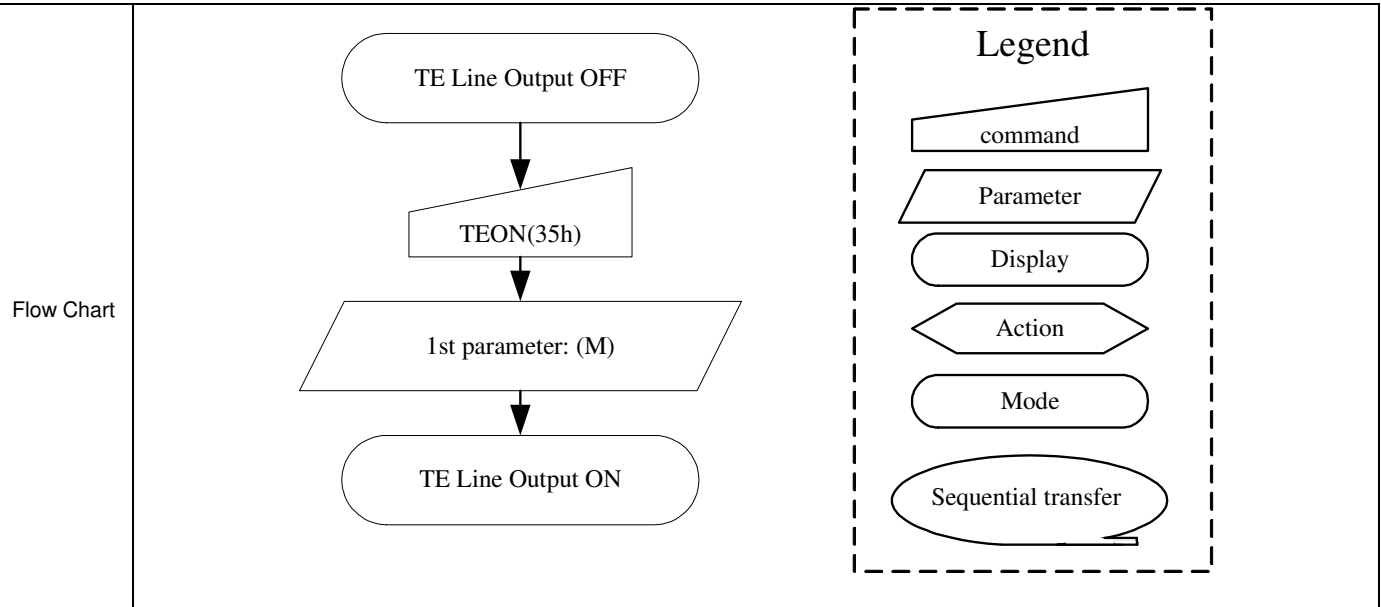
34H	TEOFF (Tearing Effect Line OFF)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	1	1	0	1	0	0	34h												
Parameter	NO PARAMETER																								
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.																								
Restriction	This command has no effect when Tearing Effect output is already OFF.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF				
	Status	Default Value																							
	Power On Sequence	OFF																							
	SW Reset	OFF																							
HW Reset	OFF																								

Flow Chart



## 14.2.28 Tearing Effect Line On (35h)

35H	TEON (Tearing Effect Line ON)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	1	1	0	1	0	1	35h												
1 <sup>st</sup> Parameter	1	1		x	x	x	x	x	x	x	x	M	00h												
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).</p> <p>When M=0:</p> <p>The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.:</p> <div><p>Vertical Time Scale</p></div> <p>When M=1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p> <div></div>																								
	<p><b>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</b></p>																								
	Restriction	This command has no effect when Tearing Effect output is already OFF.																							
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Tearing effect off &amp; M=0</td></tr><tr><td>SW Reset</td><td>Tearing effect off &amp; M=0</td></tr><tr><td>HW Reset</td><td>Tearing effect off &amp; M=0</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Tearing effect off & M=0	SW Reset	Tearing effect off & M=0	HW Reset	Tearing effect off & M=0				
Status	Default Value																								
Power On Sequence	Tearing effect off & M=0																								
SW Reset	Tearing effect off & M=0																								
HW Reset	Tearing effect off & M=0																								



## 14.2.29 Memory Access Control (36h)

36H		MADCTL (Memory Access Control)																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1		x	0	0	1	1	0	1	1	0	36h																			
1 <sup>st</sup> Parameter	1	1		x	MY	MX	MV	ML	RGB	MH	x	x	00h																			
Description	This command defines read/write scanning direction of frame memory.																															
	This command makes no change on the other driver status.																															
	Bit Assignment																															
	<table><thead><tr><th>Bit</th><th>Description</th><th>Comment</th></tr></thead><tbody><tr><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits controls MPU to memory write/read direction.</td></tr><tr><td>MX</td><td>Column Address Order</td></tr><tr><td>MV</td><td>Page/Column Selection</td></tr><tr><td>ML</td><td>Vertical Order</td><td>LCD Vertical refresh direction control</td></tr><tr><td>RGB</td><td>RGB/BGR Order</td><td>Color selector switch control 0=RGB color filter panel 1=BGR color filter panel</td></tr><tr><td>MH</td><td>Display data latch order</td><td>'1'=LCD Refresh right to left '0'=LCD Refresh left to right</td></tr></tbody></table>													Bit	Description	Comment	MY	Row Address Order	These 3 bits controls MPU to memory write/read direction.	MX	Column Address Order	MV	Page/Column Selection	ML	Vertical Order	LCD Vertical refresh direction control	RGB	RGB/BGR Order	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel	MH	Display data latch order	'1'=LCD Refresh right to left '0'=LCD Refresh left to right
	Bit	Description	Comment																													
	MY	Row Address Order	These 3 bits controls MPU to memory write/read direction.																													
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	MV	Page/Column Selection																														
	ML	Vertical Order	LCD Vertical refresh direction control																													
	RGB	RGB/BGR Order	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel																													
MH	Display data latch order	'1'=LCD Refresh right to left '0'=LCD Refresh left to right																														
<table><thead><tr><th>B5</th><th>B6</th><th>B7</th><th>Image in Frame Memory</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>0</td><td>1</td><td></td></tr><tr><td>0</td><td>1</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td>1</td><td></td></tr></tbody></table>													B5	B6	B7	Image in Frame Memory	0	0	0		0	0	1		0	1	0		0	1	1	
B5	B6	B7	Image in Frame Memory																													
0	0	0																														
0	0	1																														
0	1	0																														
0	1	1																														
<table><thead><tr><th>B5</th><th>B6</th><th>B7</th><th>Image in Frame Memory</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>0</td><td></td></tr><tr><td>1</td><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td>1</td><td></td></tr></tbody></table>													B5	B6	B7	Image in Frame Memory	1	0	0		1	0	1		1	1	0		1	1	1	
B5	B6	B7	Image in Frame Memory																													
1	0	0																														
1	0	1																														
1	1	0																														
1	1	1																														

	<div>B3 = 0</div> <div><div>Memory</div><div><div>R</div><div>G</div><div>B</div></div><div>Sent RGB</div><div>Display Panel</div><div><div>R</div><div>G</div><div>B</div></div></div> <div>B3 = 1</div> <div><div>Memory</div><div><div>R</div><div>G</div><div>B</div></div><div>Sent BGR</div><div>Display Panel</div><div><div>B</div><div>G</div><div>R</div></div></div>												
Restriction	-D1 and D0 of the 1 <sup>st</sup> parameter are set to "00" internally.												
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td></tr><tr><td>SW Reset</td><td>No Change</td></tr><tr><td>HW Reset</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td></tr></table>	Status	Default Value	Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0	SW Reset	No Change	HW Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0
Status	Default Value								
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0								
SW Reset	No Change								
HW Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0								
Flow Chart	<div><div><div>MADCTR(36h)</div><div>↓</div><div>1st parameter: (MY, MX, MV, ML, RGB, MH)</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>								

### 14.2.30 Vertical Scrolling Start Address (37h)

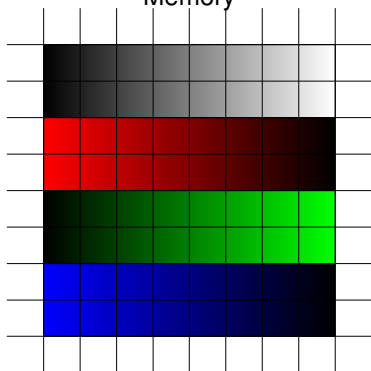
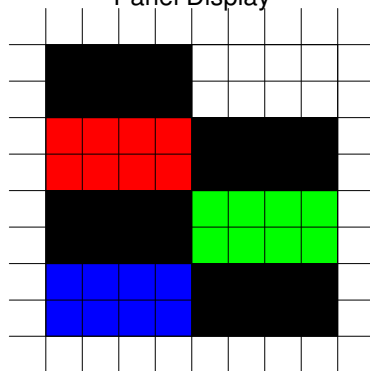
37H	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	1	1	0	1	1	1	37h
1 <sup>st</sup> Parameter	1	1		x	SSA 15	SSA 14	SSA 13	SSA 12	SSA 11	SSA 10	SSA 9	SSA 8	00h
2 <sup>nd</sup> Parameter	1	1		x	SSA 7	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	00h
Description	<p>This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.</p> <p>The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: This command Start the scrolling.</p> <p>When MADCTL ML=0 Example: GM=000, 132RGBx162 When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and Vertical Scrolling Pointer SSA='3'.</p> <div style="text-align: center;"> </div> <p>When MADCTL ML=1 Example: GM=000, 132RGBx162 When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and SSA='3'.</p> <div style="text-align: center;"> </div> <p>Note:</p> <p>When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory scan address</p> <p>When new Pointer position and Picture Data, internal system works as 128x128 and maximum scan address becomes 127 internal of 161.</p> <p>X=Don't care</p>												
Restriction	<p>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel. SSA[15:0] is based on 1-line unit.</p> <p>SSA[15:0] =0000h, 0001h, 0002h, 003h, ..., 00A1h</p>												

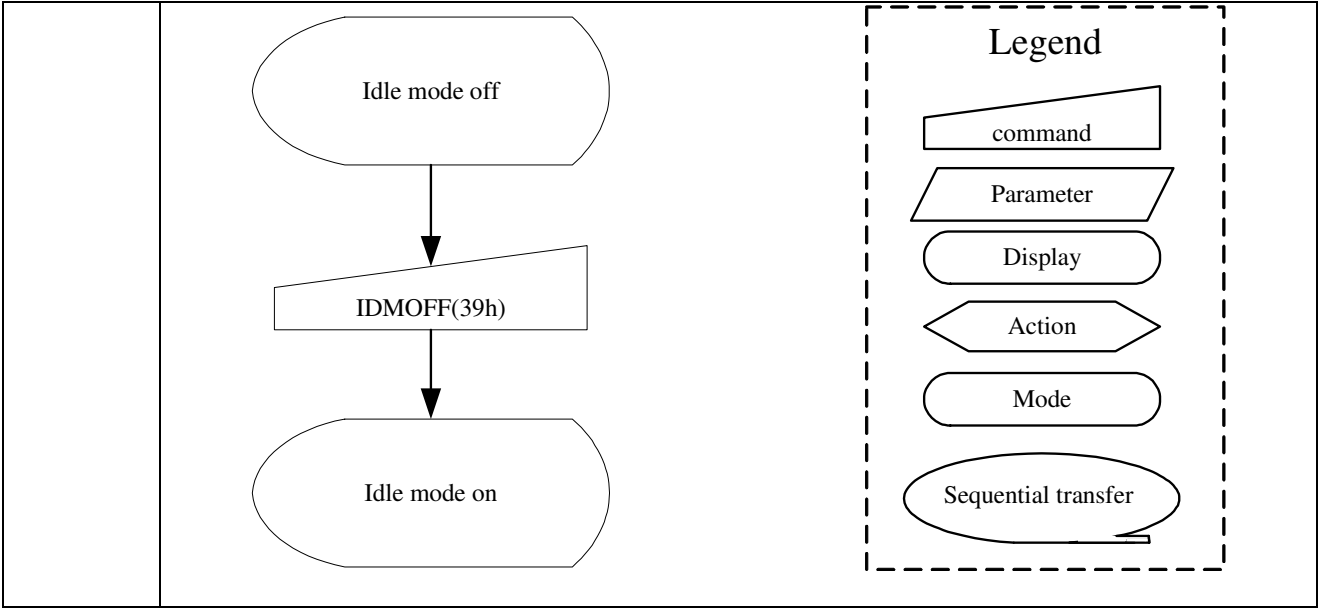
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability											
	Normal Mode On, Idle Mode Off, Sleep Out	Yes											
	Normal Mode On, Idle Mode On, Sleep Out	Yes											
	Partial Mode On, Idle Mode Off, Sleep Out	Yes											
	Partial Mode On, Idle Mode On, Sleep Out	Yes											
Sleep In	Yes												
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>SW Reset</td><td>0000h</td></tr><tr><td>HW Reset</td><td>0000h</td></tr></table>	Status	Default Value	Power On Sequence	0000h	SW Reset	0000h	HW Reset	0000h				
	Status	Default Value											
	Power On Sequence	0000h											
	SW Reset	0000h											
HW Reset	0000h												
Flow Chart	See Vertical Scrolling Definition (33h) description.												

### 14.2.31 Idle Mode Off (38h)

38H	IDMOFF (Idle Mode Off)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	0	0	1	1	1	0	0	0	38h												
Parameter	NO PARAMETER																								
Description	<p>This command is used to recover from Idle mode on.</p> <p>There will be no abnormal visible effect on the display mode change transition.</p> <p>In the Idle off mode</p> <p>1. LCD can display maximum 4096, 65K, 262K colors.</p> <p>2. Normal frame frequency is applied.</p> <p>X = don't care</p>																								
Restriction	This command has no effect when module is already in idle off mode.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off				
Status	Default Value																								
Power On Sequence	Idle Mode Off																								
SW Reset	Idle Mode Off																								
HW Reset	Idle Mode Off																								
Flow Chart	<div><div><div>Idle mode on</div><div></div><div>IDMOFF(38h)</div><div></div><div>Idle mode off</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

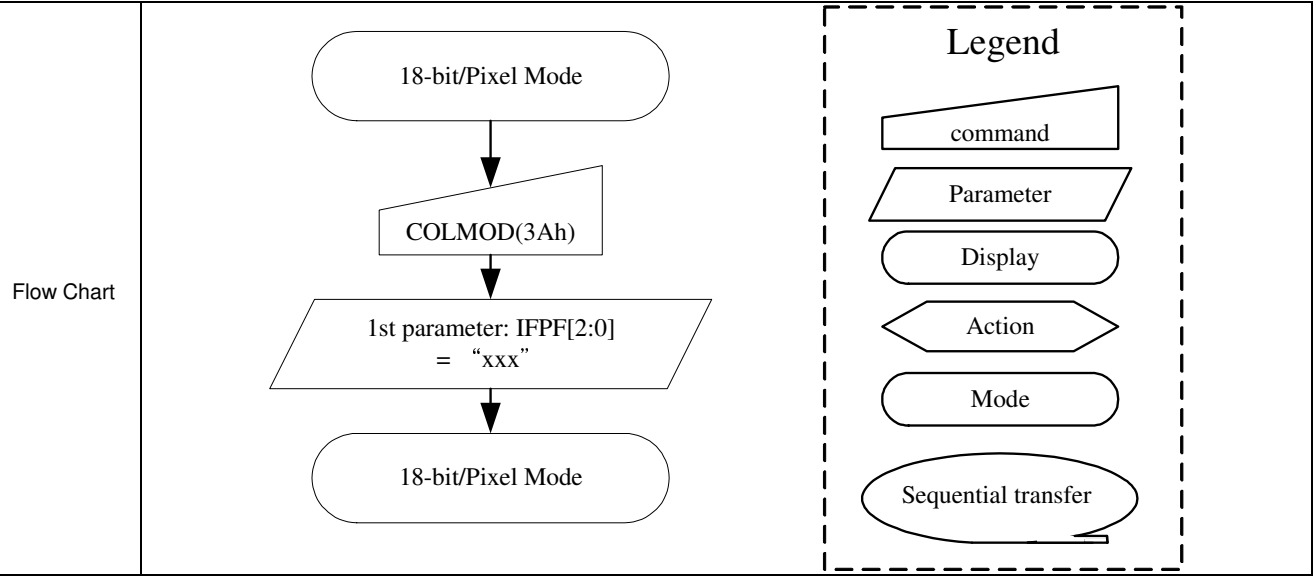
### 14.2.32 Idle Mode On (39h)

39H	IDMON (Idle Mode On)																																																
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1		x	0	0	1	1	1	0	0	1	39h																																				
Parameter	NO PARAMETER																																																
Description	<p>This command is used to enter into Idle mode on.</p> <p>There will be no abnormal visible effect on the display mode change transition.</p> <p>In the Idle mode,</p> <ol style="list-style-type: none"><li>Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.</li><li>8-Color mode frame frequency is applied.</li><li>Exit from IDMON by Idle Mode Off(38h) command.</li></ol>																																																
	<div><div><p>Memory</p></div><div><p>Panel Display</p></div></div> <table><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></table>														R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX
		R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0																																													
	Black	0XXXXX	0XXXXX	0XXXXX																																													
Blue	0XXXXX	0XXXXX	1XXXXX																																														
Red	1XXXXX	0XXXXX	0XXXXX																																														
Magenta	1XXXXX	0XXXXX	1XXXXX																																														
Green	0XXXXX	1XXXXX	0XXXXX																																														
Cyan	0XXXXX	1XXXXX	1XXXXX																																														
Yellow	1XXXXX	1XXXXX	0XXXXX																																														
White	1XXXXX	1XXXXX	1XXXXX																																														
Restriction	This command has no effect when module is already in idle on mode.																																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
Status	Availability																																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																																
Sleep In	Yes																																																
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr></table>													Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off																														
Status	Default Value																																																
Power On Sequence	Idle Mode Off																																																
SW Reset	Idle Mode Off																																																
Flow Chart																																																	



### 14.2.33 Interface Pixel Format (3Ah)

39H	IDMON (Idle Mode On)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	0	0	1	1	1	0	1	0	3Ah
1 <sup>st</sup> Parameter	1	1		x	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h
Description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:												
	Bit		Description					Value					
	VIPF3		RGB Interface Color Format					“0101”=16 bit/pixel (1 times data transfer)					
	VIPF2							“0110”=18 bit/pixel (1 times data transfer)					
	VIPF1							“1110”=18 bit/pixel (3 times data transfer)					
	VIPF0							The others = not defined					
	D3							“0” (Not Used)					
	IFPF2		Control Interface Color Format					“011”=12 bit/pixel					
	IFPF1							“101”=16 bit/pixel					
	IFPF0							“110”=18 bit/pixel					
							The others = not defined						
Note													
1.In 12-bits/Pixel, 16-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.													
2. When VIPF[3:0]=1110, 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.													
X = don't care													
Restriction	There is no visible effect until the Frame Memory is written to.												
Register Availability													
Default													



### 14.2.37 Frame Rate Control (In normal mode/Full colors) (B1h)

B1h	Frame Rate Control(In normal mode/Full colors)																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		1	0	1	1	0	0	0	1	B1h												
1 <sup>st</sup> Parameter	1	1		x	x	x	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	x												
2 <sup>nd</sup> Parameter	1	1		x	x	VPA5	VPA4	VPA3	VPA2	VPA1	VPA0	x												
Description	<p>Sets the division ratio for internal clocks of Normal mode at CPU interface mode.</p> <p>DIVA[4:0]: division ratio for internal clocks when Normal mode.</p> <p>VPA[5:0]: VS porch for internal clocks when Normal mode</p> $Frame\_rate = \frac{200kHz}{(Line + VPA[5 : 0])(DIVA[4 : 0] + 4)}$ <p>(1) When GM=101(132*132)</p> <p>In Normal mode, line=132, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=62.7Hz</p> <p>(2) When GM=100(130*130)</p> <p>In Normal mode, line=130, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=63.5Hz</p> <p>(3) When GM=011(128*160)</p> <p>In Normal mode, line=160, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61.7Hz</p> <p>(4) When GM=010(120*160)</p> <p>In Normal mode, line=160, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61.7Hz</p> <p>(5) When GM=001(128*128)</p> <p>In Normal mode, line=128, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=64.4Hz</p> <p>(6) When GM=000(132*162)</p> <p>In Normal mode, line=162, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61Hz</p>																							
Restriction	-																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							

Default	<div>(1) When GM=000(132*162), GM=011(128*160) or GM=010(120*160)</div> <table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIVA[4:0]</th><th>VPA[5:0]</th></tr><tr><td>Power On Sequence</td><td>0Eh/14d</td><td>14h/20d</td></tr><tr><td>S/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr><tr><td>H/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr></table>	Status	Default Value		DIVA[4:0]	VPA[5:0]	Power On Sequence	0Eh/14d	14h/20d	S/W Reset	0Eh/14d	14h/20d	H/W Reset	0Eh/14d	14h/20d
	Status		Default Value												
DIVA[4:0]		VPA[5:0]													
Power On Sequence	0Eh/14d	14h/20d													
S/W Reset	0Eh/14d	14h/20d													
H/W Reset	0Eh/14d	14h/20d													
	<div>(2) When GM=001(128*128), GM=100(130*130), GM=101(132*132)</div> <table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIVA[4:0]</th><th>VPA[5:0]</th></tr><tr><td>Power On Sequence</td><td>11h/17d</td><td>11h/17d</td></tr><tr><td>S/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr><tr><td>H/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr></table>	Status	Default Value		DIVA[4:0]	VPA[5:0]	Power On Sequence	11h/17d	11h/17d	S/W Reset	11h/17d	11h/17d	H/W Reset	11h/17d	11h/17d
Status	Default Value														
	DIVA[4:0]	VPA[5:0]													
Power On Sequence	11h/17d	11h/17d													
S/W Reset	11h/17d	11h/17d													
H/W Reset	11h/17d	11h/17d													
Flow Chart	<div><div>RGBCTR1(B1h)</div><div>↓</div><div>1st parameter: DIVA[4:0] 2nd parameter: VPA[4:0]</div></div> <div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>														

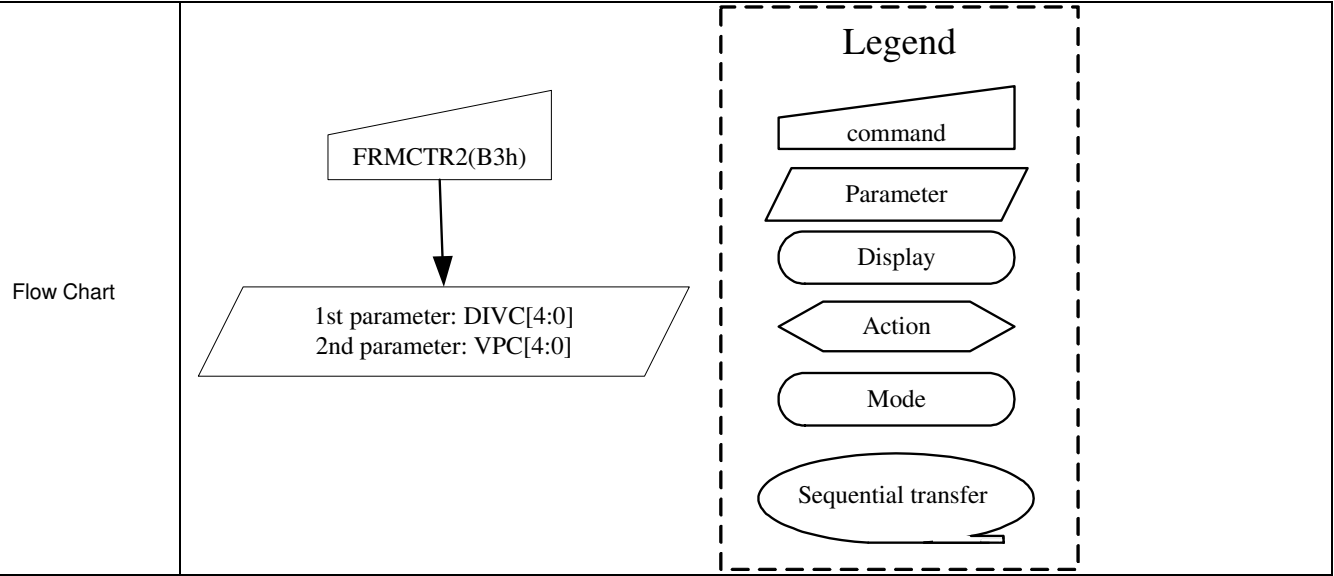
### 14.2.38 Frame Rate Control(In Idle mode/8-colors) (B2h)

B2h	Frame Rate Control(In Idle mode/Full colors)																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		1	0	1	1	0	0	1	0	B2h												
1 <sup>st</sup> Parameter	1	1		x	x	x	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0	x												
2 <sup>nd</sup> Parameter	1	1		x	x	VPB5	VPB4	VPB3	VPB2	VPB1	VPB0	x												
Description	<p>Sets the division ratio for internal clocks of Idle mode at CPU interface mode.</p> <p>DIVB[4:0]: division ratio for internal clocks when Idle mode.</p> <p>VPB[5:0]: VS porch for internal clocks when Idle mode</p> $Frame\_rate = \frac{200kHz}{(Line + VPB[5 : 0])(DIVB[4 : 0] + 4)}$ <p>(1) When GM=101(132*132)</p> <p>In Normal mode, line=132, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=62.7Hz</p> <p>(2) When GM=100(130*130)</p> <p>In Normal mode, line=130, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=63.5Hz</p> <p>(3) When GM=011(128*160)</p> <p>In 8-color mode, line=160, Default value DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61.7Hz</p> <p>(4) When GM=010(120*160)</p> <p>In 8-color I mode, line=160, Default value DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61.7Hz</p> <p>(5) When GM=001(128*128)</p> <p>In 8-color mode, line=128, Default value DIVB[4:0]=17, VPB[5:0]=20, Frame rate=64.4Hz</p> <p>(6) When GM=000(132*162)</p> <p>In 8-color mode, line=162, Default value DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61Hz</p>																							
Restriction	-																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							

Default	<div>(1) When GM=000(132*162), GM=011(128*160) or GM=010(120*160)</div> <table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIVB[4:0]</th><th>VPB[5:0]</th></tr><tr><td>Power On Sequence</td><td>0Eh/14d</td><td>14h/20d</td></tr><tr><td>S/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr><tr><td>H/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr></table> <div>(2) When GM=001(128*128), GM=100(130*130), GM=101(132*132)</div> <table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIVB[4:0]</th><th>VPB[5:0]</th></tr><tr><td>Power On Sequence</td><td>11h/17d</td><td>11h/17d</td></tr><tr><td>S/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr><tr><td>H/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr></table>	Status	Default Value		DIVB[4:0]	VPB[5:0]	Power On Sequence	0Eh/14d	14h/20d	S/W Reset	0Eh/14d	14h/20d	H/W Reset	0Eh/14d	14h/20d	Status	Default Value		DIVB[4:0]	VPB[5:0]	Power On Sequence	11h/17d	11h/17d	S/W Reset	11h/17d	11h/17d	H/W Reset	11h/17d	11h/17d
Status	Default Value																												
	DIVB[4:0]	VPB[5:0]																											
Power On Sequence	0Eh/14d	14h/20d																											
S/W Reset	0Eh/14d	14h/20d																											
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	DIVB[4:0]	VPB[5:0]																											
Power On Sequence	11h/17d	11h/17d																											
S/W Reset	11h/17d	11h/17d																											
H/W Reset	11h/17d	11h/17d																											
Flow Chart	<div><div>FRMCTR2(B2h)</div><div>↓</div><div>1st parameter: DIVB[4:0] 2nd parameter: VPB[4:0]</div></div> <div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																												

### 14.2.39 Frame Rate Control(In Partial mode/full colors) (B3h)

B3h	Frame Rate Control(In Partial mode/Full colors)																																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1		1	0	1	1	0	0	1	1	B3h																												
1 <sup>st</sup> Parameter	1	1		x	x	x	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0	x																												
2 <sup>nd</sup> Parameter	1	1		x	x	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	x																												
Description	<p>Sets the division ratio for internal clocks of Partial mode at CPU interface mode.</p> <p>DIVB[4:0]: division ratio for internal clocks when Partial mode.</p> <p>VPB[5:0]: VS porch for internal clocks when Partial mode</p> $Frame\_rate = \frac{200kHz}{(Line + VPC[5 : 0])(DIVC[4 : 0] + 4)}$ <p>(1) When GM=101(132*132)</p> <p>In Normal mode, line=132, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=62.7Hz</p> <p>(2) When GM=100(130*130)</p> <p>In Normal mode, line=130, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=63.5Hz</p> <p>(3) When GM=011(128*160)</p> <p>In Partial mode, line=160, Default value DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61.7Hz</p> <p>(4) When GM=010(120*160)</p> <p>In Partial mode, line=160, Default value DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61.7Hz</p> <p>(5) When GM=001(128*128)</p> <p>In Partial mode, line=128, Default value DIVC[4:0]=17, VPC[5:0]=20, Frame rate=64.4Hz</p> <p>(6) When GM=000(132*162)</p> <p>In Partial mode, line=162, Default value DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61Hz</p>																																							
Restriction	-																																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																
Status	Availability																																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																																							
Sleep In	Yes																																							
Default	<p>(1) When GM=000(132*162), GM=011(128*160) or GM=010(120*160)</p> <table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIVC4:0]</th><th>VPC[5:0]</th></tr><tr><td>Power On Sequence</td><td>0Eh/14d</td><td>14h/20d</td></tr><tr><td>S/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr><tr><td>H/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr></table> <p>(3) When GM=001(128*128), GM=100(130*130), GM=101(132*132)</p> <table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIVB[4:0]</th><th>VPB[5:0]</th></tr><tr><td>Power On Sequence</td><td>11h/17d</td><td>11h/17d</td></tr><tr><td>S/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr><tr><td>H/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr></table>												Status	Default Value		DIVC4:0]	VPC[5:0]	Power On Sequence	0Eh/14d	14h/20d	S/W Reset	0Eh/14d	14h/20d	H/W Reset	0Eh/14d	14h/20d	Status	Default Value		DIVB[4:0]	VPB[5:0]	Power On Sequence	11h/17d	11h/17d	S/W Reset	11h/17d	11h/17d	H/W Reset	11h/17d	11h/17d
Status	Default Value																																							
	DIVC4:0]	VPC[5:0]																																						
Power On Sequence	0Eh/14d	14h/20d																																						
S/W Reset	0Eh/14d	14h/20d																																						
H/W Reset	0Eh/14d	14h/20d																																						
Status	Default Value																																							
	DIVB[4:0]	VPB[5:0]																																						
Power On Sequence	11h/17d	11h/17d																																						
S/W Reset	11h/17d	11h/17d																																						
H/W Reset	11h/17d	11h/17d																																						



#### 14.2.40 Display Inversion Control (B4h)

B4h	Display Inversion Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	1	0	1	1	0	1	0	0	B4h
1 <sup>st</sup> Parameter	1	1		x	0	0	0	0	0	NLA	NLB	NLC	02H

-Display Inversion mode control

-NLA: Inversion setting in full colors normal mode(Normal mode on)

NLA	Inversion setting in full colors normal mode
0	Line Inversion
1	Frame Inversion

-NLB: Inversion setting in Idle mode(Idle mode on)

Description

NLB	Inversion setting in Idle mode
0	Line Inversion
1	Frame Inversion

-NLC: Inversion setting in full colors partial mode(Partial mode on/Idle mode off)

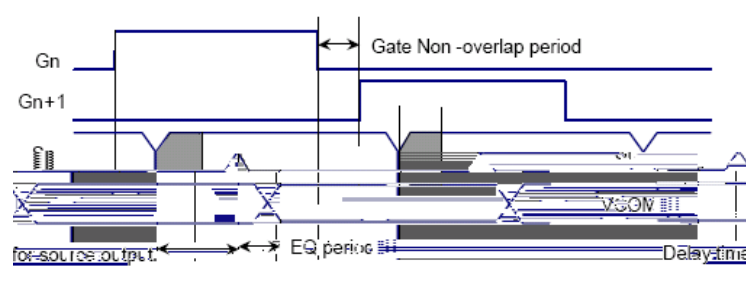
NLC	Inversion setting in full colors partial mode
0	Line Inversion
1	Frame Inversion

#### 14.2.41 RGB Interface Blanking Porch setting (B5h)

B5h	RGB Interface Blanking Porch setting																																
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1		x	1	0	1	1	0	1	0	1	B5h																				
1 <sup>st</sup> Parameter	1	1		x	x	x	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	08h																				
2 <sup>nd</sup> Parameter	1	1		x	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	03h																				
3 <sup>rd</sup> Parameter	1	1		x	x	x	x	x	x	x	VBP9	VBP8	00h																				
Description	Vertical and Horizontal back porch control when RGB I/F mode2(RCM[1:0]=11)																																
	HBP[5:0]: Set the delay period from falling edge of HSYNC signal to first vali data.																																
	<table><tr><td>HBP[5:0]</td><td>No.of clock cycle of DOTCLK</td></tr><tr><td>00d</td><td>2</td></tr><tr><td>01d</td><td>3</td></tr><tr><td>02d</td><td>4</td></tr><tr><td>03d</td><td>5</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>(SETP1)</td></tr><tr><td>:</td><td>:</td></tr><tr><td>62d</td><td>64</td></tr><tr><td>63d</td><td>65</td></tr></table>													HBP[5:0]	No.of clock cycle of DOTCLK	00d	2	01d	3	02d	4	03d	5	:	:	:	(SETP1)	:	:	62d	64	63d	65
	HBP[5:0]	No.of clock cycle of DOTCLK																															
	00d	2																															
	01d	3																															
	02d	4																															
	03d	5																															
	:	:																															
	:	(SETP1)																															
	:	:																															
	62d	64																															
	63d	65																															
	VBP[9:0]: Set the delay period from falling edge of VSYNC signal to first valid line.																																
	<table><tr><td>VBP[9:0]</td><td>No. of clock cycle of HSYNC</td></tr><tr><td>00d</td><td>(invalid)</td></tr><tr><td>01d</td><td>1</td></tr><tr><td>02d</td><td>2</td></tr><tr><td>03d</td><td>3</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>(STEP1):</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1022d</td><td>1022</td></tr></table>													VBP[9:0]	No. of clock cycle of HSYNC	00d	(invalid)	01d	1	02d	2	03d	3	:	:	:	(STEP1):	:	:	1022d	1022		
VBP[9:0]	No. of clock cycle of HSYNC																																
00d	(invalid)																																
01d	1																																
02d	2																																
03d	3																																
:	:																																
:	(STEP1):																																
:	:																																
1022d	1022																																
Restriction	-																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
	Status	Availability																															
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
	Normal Mode On, Idle Mode On, Sleep Out	Yes																															
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																															
	Partial Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In	Yes																																

Default		Default Value	
		Status	
		HBP[5:0]	VBP[9:0]
		Power On Sequence	08h
		S/W Reset	08h
Flow Chart		Legend	

### 14.2.43 Display Fuction set 5 (B6h)

B6h	RGB Interface Blanking Porch setting																																																																																				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																								
Command	0	1		x	1	0	1	1	0	1	1	0	B6h																																																																								
1 <sup>st</sup>	1	1		x	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ2	07h																																																																								
2 <sup>nd</sup>	1	1		x	0	0	0	0	0	PTG0	PT1	PT0	02h																																																																								
Description	<p>-1<sup>st</sup> parameter: Set output waveform relation.</p> <p>-NO[1:0]: Set the amount for non-overlap of the gate output</p> <table><tr><th colspan="2">NO[1:0]</th><th colspan="2">Amount of non-overlap of the gate output</th></tr><tr><th colspan="2"></th><th colspan="2">Refer the Internal oscillator</th></tr><tr><td>00</td><td>0</td><td colspan="2">4 clock cycle</td></tr><tr><td>01</td><td>1</td><td colspan="2">5 clock cycle</td></tr><tr><td>10</td><td>2</td><td colspan="2">6 clock cycle</td></tr><tr><td>11</td><td>3</td><td colspan="2">7 clock cycle</td></tr></table> <p>-SDT[1:0]: Set delay amount from gate signal falling edge to the source output.</p> <table><tr><th colspan="2">SDT[1:0]</th><th colspan="2">Amount of non-overlap of the source output</th></tr><tr><th colspan="2"></th><th colspan="2">Refer the Internal oscillator</th></tr><tr><td>00</td><td>0</td><td colspan="2">4 clock cycle</td></tr><tr><td>01</td><td>1</td><td colspan="2">4 clock cycle</td></tr><tr><td>10</td><td>2</td><td colspan="2">4.5 clock cycle</td></tr><tr><td>11</td><td>3</td><td colspan="2">5.5 clock cycle</td></tr></table> <p>-EQ[1:0]: Set the Equalizing period.</p> <table><tr><th colspan="2">EQ[1:0]</th><th colspan="2">EQ period</th></tr><tr><th colspan="2"></th><th colspan="2">Refer the Internal oscillator</th></tr><tr><td>00</td><td>0</td><td colspan="2">No EQ</td></tr><tr><td>01</td><td>1</td><td colspan="2">0.5 clock cycle</td></tr><tr><td>10</td><td>2</td><td colspan="2">1 clock cycle</td></tr><tr><td>11</td><td>3</td><td colspan="2">1.5 clock cycle</td></tr></table>  <p>The diagram illustrates the timing relationship between the gate signal (Gn, Gn+1) and the source output. It shows the Gate Non-overlap period, the EQ period (Equalizing period), and the Delay time for the source output. The source output is shown as a series of pulses, with the EQ period and Delay time indicated by arrows.</p>													NO[1:0]		Amount of non-overlap of the gate output				Refer the Internal oscillator		00	0	4 clock cycle		01	1	5 clock cycle		10	2	6 clock cycle		11	3	7 clock cycle		SDT[1:0]		Amount of non-overlap of the source output				Refer the Internal oscillator		00	0	4 clock cycle		01	1	4 clock cycle		10	2	4.5 clock cycle		11	3	5.5 clock cycle		EQ[1:0]		EQ period				Refer the Internal oscillator		00	0	No EQ		01	1	0.5 clock cycle		10	2	1 clock cycle		11	3	1.5 clock cycle	
	NO[1:0]		Amount of non-overlap of the gate output																																																																																		
			Refer the Internal oscillator																																																																																		
	00	0	4 clock cycle																																																																																		
	01	1	5 clock cycle																																																																																		
	10	2	6 clock cycle																																																																																		
	11	3	7 clock cycle																																																																																		
	SDT[1:0]		Amount of non-overlap of the source output																																																																																		
			Refer the Internal oscillator																																																																																		
	00	0	4 clock cycle																																																																																		
01	1	4 clock cycle																																																																																			
10	2	4.5 clock cycle																																																																																			
11	3	5.5 clock cycle																																																																																			
EQ[1:0]		EQ period																																																																																			
		Refer the Internal oscillator																																																																																			
00	0	No EQ																																																																																			
01	1	0.5 clock cycle																																																																																			
10	2	1 clock cycle																																																																																			
11	3	1.5 clock cycle																																																																																			
<p>-2<sup>nd</sup> parameter: Set the output waveform in non-display area.</p> <p>-PTG[0]: Determine gate output in a non-display area in the partial mode.</p> <table><tr><th colspan="2">PTG[0]</th><th colspan="2">Gate output in a non-display area</th></tr><tr><td>0</td><td>0</td><td colspan="2">Normal scan</td></tr><tr><td>1</td><td>1</td><td colspan="2">Fix on VGL</td></tr></table>													PTG[0]		Gate output in a non-display area		0	0	Normal scan		1	1	Fix on VGL																																																														
PTG[0]		Gate output in a non-display area																																																																																			
0	0	Normal scan																																																																																			
1	1	Fix on VGL																																																																																			

	-PT[1:0]: Determine Source/VCOM output in a non-display area in the partial mode																																			
PT[1:0]		Source output on non-display area		VCOM output on non-display area																																
		Positive	Negative	Positive	Negative																															
00	0	V63	V0	VCOMH	VCOML																															
01	1	V0	V63	VCOMH	VCOML																															
10	2	AGND	AGND	AGND	AGND																															
11	3	Hi-z	Hi-z	AGND	AGND																															
Restriction	If this register not using the register need be reserved.																																			
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>						Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																		
Status	Availability																																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																																			
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																			
Partial Mode On, Idle Mode On, Sleep Out	Yes																																			
Sleep In	Yes																																			
Default	<table><tr><th rowspan="2">Status</th><th colspan="4">Default Value</th><th></th></tr><tr><th>NO[1:0]</th><th>STD[1:0]</th><th>EQ[1:0]</th><th>PTG[1:0]</th><th>PT[1:0]</th></tr><tr><td>Power On Sequence</td><td>0d</td><td>1d</td><td>2d</td><td>0d</td><td>2d</td></tr><tr><td>S/W Reset</td><td>0d</td><td>1d</td><td>2d</td><td>0d</td><td>2d</td></tr><tr><td>H/W Reset</td><td>0d</td><td>1d</td><td>2d</td><td>0d</td><td>2d</td></tr></table>						Status	Default Value					NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]	Power On Sequence	0d	1d	2d	0d	2d	S/W Reset	0d	1d	2d	0d	2d	H/W Reset	0d	1d	2d	0d	2d	
Status	Default Value																																			
	NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]																															
Power On Sequence	0d	1d	2d	0d	2d																															
S/W Reset	0d	1d	2d	0d	2d																															
H/W Reset	0d	1d	2d	0d	2d																															

command

Parameter

Flow Chart

## 14.2.42 Source Driver Direction Control (B7h)

B7h		Display Inversion Control																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1		x	1	0	1	1	0	1	1	1	B7h											
1 <sup>st</sup> Parameter	1	1		x	0	0	0	0	0	0	0	CRL	00h											
Description	-CRL: Source output direction select register																							
	CRL		Module source output direction																					
			GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'																
	0	S1 -> S396	S7 -> S396	S7 -> S390	S7 -> S366	S7 -> S390	S1 -> S396																	
		1	S1 -> S396	S396 -> S7	S390 ->S7	S366 -> S7	S390 -> S7	S396 -> S1																
Restriction	If this register not using the register need be reserved.																							
Register Availability																								
	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																						
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
	Normal Mode On, Idle Mode On, Sleep Out	Yes																						
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default																								
	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>CRL</th></tr><tr><td>Power On Sequence</td><td>0d</td></tr><tr><td>S/W Reset</td><td>0d</td></tr><tr><td>H/W Reset</td><td>0d</td></tr></table>												Status	Default Value	CRL	Power On Sequence	0d	S/W Reset	0d	H/W Reset	0d			
	Status	Default Value																						
		CRL																						
	Power On Sequence	0d																						
S/W Reset	0d																							
H/W Reset	0d																							
Flow Chart																								
	<div><div><div>SDOCTR(B7h)</div><div></div><div>1st Parameter: CRL</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																							

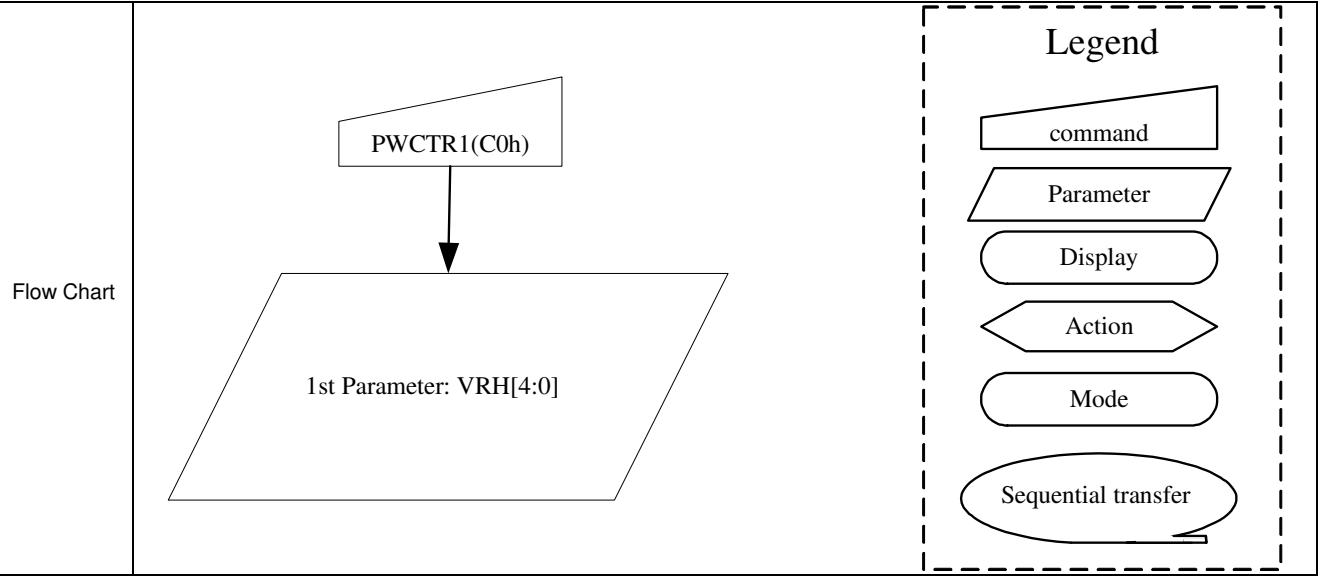


14.2.43 Gate Driver Direction Control (B8h)

B8h	Display Inversion Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	1	0	1	1	1	0	0	0	B8h
<sup>1st</sup> Parameter	1	1		x	0	0	0	0	0	0	0	CTB	00h

## 14.2.44 Power\_Control1 (C0h)

C0H	Power_Control1													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1		x	1	1	0	0	0	0	0	0	C0h	
1 <sup>st</sup> Parameter	1	1		x	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	x	
2 <sup>nd</sup> Parameter	1	1		x	0	0	0	0	0	0	VC2	VC1	VC0	02h
Description	Set the GVDD and voltage													
	VRH[4:0]			GVDD										
	00000	0	5.00											
	00001	1	4.75											
	00010	2	4.70											
	00011	3	4.65											
	00100	4	4.60											
	00101	5	4.55											
	00110	6	4.50											
	00111	7	4.45											
	01000	8	4.40											
	01001	9	4.35											
	01010	10	4.30											
	01011	11	4.25											
	01100	12	4.20											
	01101	13	4.15											
	01110	14	4.10											
	01111	15	4.05											
	10000	16	4.00											
	10001	17	3.95											
	10010	18	3.90											
	10011	19	3.85											
	10100	20	3.80											
	10101	21	3.75											
	10110	22	3.70											
	10111	23	3.65											
	11000	24	3.60											
	11001	25	3.55											
	11010	26	3.50											
	11011	27	3.45											
	11100	28	3.40											
	11101	29	3.35											
	11110	30	3.25											
	11111	31	3.00											
	VC[2:0]													
	VC1													
000	0	2.75												
001	1	2.70												
010	2	2.65												
011	3	2.60												
100	4	2.55												
101	5	2.50												
110	6	2.45												
111	7	2.40												
Restriction														
Register Availability														
Default														



#### 14.2.45 Power\_Control2 (C1h)

C1H	Power_Control 2																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	1	1	0	0	0	0	0	1	C1h												
1 <sup>st</sup> Parameter	1	1		x	0	0	0	0	0	BT2	BT1	BT0	07h												
Description	Set the AVDD, VCL, VGH and VGL supply power level.																								
	BT[2:0]		AVDD		VCL		VGH		VGL																
	010	2	2xVCI		-1xVCI1		5xVCI		-5xVCI																
	011	3	2xVCI		-1xVCI1		6xVCI		-5xVCI																
	100	4	2xVCI		-1xVCI1		5xVCI		-6xVCI																
	101	5	2xVCI		-1xVCI1		6xVCI		-6xVCI																
Restriction	If this register not using the register need be reserved. The deviation value of VGH/VGL between with Measurement and Specification VGH-VGL <= 32V																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><td>BT[2:0]</td></tr><tr><td>Power On Sequence</td><td>7d</td></tr><tr><td>SW Reset</td><td>7d</td></tr><tr><td>HW Reset</td><td>7d</td></tr></table>													Status	Default Value	BT[2:0]	Power On Sequence	7d	SW Reset	7d	HW Reset	7d			
Status	Default Value																								
	BT[2:0]																								
Power On Sequence	7d																								
SW Reset	7d																								
HW Reset	7d																								
Flow Chart	<div><div><div>PWCTR2(C1h)</div><div></div><div>1st Parameter: BT[2:0]</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

## 14.2.46 Power\_Control 3 (C2h)

C2H	Power_Control 3																																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1		x	1	1	0	0	0	0	1	0	C2h																											
1 <sup>st</sup> Parameter	1	1		x	0	0	0	0	0	APA2	APA1	APA0	00h																											
Description	Set the amount of current in Operation amplifier in normal mode/full colors.																																							
	Adjust the amount of fixed current from the fixed current sources in the operational amplifier for the source driver.																																							
	<table><tr><th colspan="2">APA[2:0]</th><th>Amount of Current in Operational Amplifier</th></tr><tr><td>000</td><td>0</td><td>Least</td></tr><tr><td>001</td><td>1</td><td>Small</td></tr><tr><td>010</td><td>2</td><td>Medium Low</td></tr><tr><td>011</td><td>3</td><td>Medium</td></tr><tr><td>100</td><td>4</td><td>Medium High</td></tr><tr><td>101</td><td>5</td><td>Large</td></tr><tr><td>110</td><td>6</td><td>Reserved</td></tr><tr><td>111</td><td>7</td><td>Reserved</td></tr></table>													APA[2:0]		Amount of Current in Operational Amplifier	000	0	Least	001	1	Small	010	2	Medium Low	011	3	Medium	100	4	Medium High	101	5	Large	110	6	Reserved	111	7	Reserved
	APA[2:0]		Amount of Current in Operational Amplifier																																					
	000	0	Least																																					
	001	1	Small																																					
	010	2	Medium Low																																					
	011	3	Medium																																					
	100	4	Medium High																																					
	101	5	Large																																					
110	6	Reserved																																						
111	7	Reserved																																						
Restriction	If some parameter of the register is not use the register need to be reserved.																																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes															
Status	Availability																																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																																							
Sleep In	Yes																																							
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><td>APA[2:0]</td></tr><tr><td>Power On Sequence</td><td>0d</td></tr><tr><td>SW Reset</td><td>0d</td></tr><tr><td>HW Reset</td><td>0d</td></tr></table>													Status	Default Value	APA[2:0]	Power On Sequence	0d	SW Reset	0d	HW Reset	0d																		
Status	Default Value																																							
	APA[2:0]																																							
Power On Sequence	0d																																							
SW Reset	0d																																							
HW Reset	0d																																							
Flow Chart	<div><div><div>PWCTR3(C2h)</div><div></div><div>1st Parameter: APA[2:0]</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																																							

## 14.2.47 Power\_Control 4 (C3h)

C3H	Power_Control 4(in Idle mode / 8 colors)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	1	1	0	0	0	0	1	1	C3h
1 <sup>st</sup> Parameter	1	1		x	0	0	0	0	0	APB2	APB1	APB0	00h
Description	Set the amount of current in Operational amplifier in Idle mode/8-colors												
	Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.												
	APB[2:0]		Amount of Current in Operational Amplifier										
	000	0	Least										
	001	1	Small										
	010	2	Medium Low										
	011	3	Medium										
	100	4	Medium High										
	101	5	Large										
	110	6	Reserved										
111	7	Reserved											
Restriction	If some parameter of the register not use the register need to be reserved.												
Register Availability													
	Status											Availability	
	Normal Mode On, Idle Mode Off, Sleep Out											Yes	
	Normal Mode On, Idle Mode On, Sleep Out											Yes	
	Partial Mode On, Idle Mode Off, Sleep Out											Yes	
	Partial Mode On, Idle Mode On, Sleep Out											Yes	
Default													
	Status											Default Value	
												APB[2:0]	
	Power On Sequence											0d	
	SW Reset											0d	
HW Reset											0d		
Flow Chart													
	<div><div>PWCTR4(C3h)</div><div></div><div>1st Parameter: APB[2:0]</div></div>											<div>Legend</div> <div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div>	

## 14.2.48 Power\_Control 5 (C4h)

C4H	Power Control 5(in Partial mode/full mode)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	1	1	0	0	0	1	0	0	C4h												
1 <sup>st</sup> Parameter	1	1		x	0	0	0	0	0	APC2	APC1	APC1	01h												
Description	Set the amount of current in Operational amplifier in Partial mode/full-colors																								
	Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.																								
	APC[2:0]		Amount of Current in Operational Amplifier																						
	000	0	Least																						
	001	1	Small																						
	010	2	Medium Low																						
	011	3	Medium																						
	100	4	Medium High																						
	101	5	Large																						
	110	6	Reserved																						
111	7	Reserved																							
Restriction	If some parameter of the register not use the register need to be reserved.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><td>APC[2:0]</td></tr><tr><td>Power On Sequence</td><td>1d</td></tr><tr><td>SW Reset</td><td>1d</td></tr><tr><td>HW Reset</td><td>1d</td></tr></table>													Status	Default Value	APC[2:0]	Power On Sequence	1d	SW Reset	1d	HW Reset	1d			
	Status	Default Value																							
		APC[2:0]																							
	Power On Sequence	1d																							
	SW Reset	1d																							
HW Reset	1d																								
Flow Chart	<div><div><div>PWCTR5(C4h)</div><div></div><div>1st Parameter: APC[2:0]</div></div><div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

## 14.2.49 VCOM\_Control 1 (C5h)

C5H	VCOM_Control1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	1	1	0	0	0	1	0	1	C5h
1 <sup>st</sup> Parameter	1	1		x	x	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	-
2 <sup>nd</sup> Parameter	1	1		x	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0	-
Description	Set VCOMH Voltage												
	VMH[6:0]		VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH	VMH[6:0]	VCOMH		
	0000000	0	2.500	0011011	27	3.175	0110110	54	3.850	1010001	81	4.525	
	0000001	1	2.525	0011100	28	3.200	0110111	55	3.875	1010010	82	4.550	
	0000010	2	2.550	0011101	29	3.225	0111000	56	3.900	1010011	83	4.575	
	0000011	3	2.575	0011110	30	3.250	0111001	57	3.925	1010100	84	4.600	
	0000100	4	2.600	0011111	31	3.275	0111010	58	3.950	1010101	85	4.625	
	0000101	5	2.625	0100000	32	3.300	0111011	59	3.975	1010110	86	4.650	
	0000110	6	2.650	0100001	33	3.325	0111100	60	4.000	1010111	87	4.675	
	0000111	7	2.675	0100010	34	3.350	0111101	61	4.025	1011000	88	4.700	
	0001000	8	2.700	0100011	35	3.375	0111110	62	4.050	1011001	89	4.725	
	0001001	9	2.725	0100100	36	3.400	0111111	63	4.075	1011010	90	4.750	
	0001010	10	2.750	0100101	37	3.425	1000000	64	4.100	1011011	91	4.775	
	0001011	11	2.775	0100110	38	3.450	1000001	65	4.125	1011100	92	4.800	
	0001100	12	2.800	0100111	39	3.475	1000010	66	4.150	1011101	93	4.825	
	0001101	13	2.825	0101000	40	3.500	1000011	67	4.175	1011110	94	4.850	
	0001110	14	2.850	0101001	41	3.525	1000100	68	4.200	1011111	95	4.875	
	0001111	15	2.875	0101010	42	3.550	1000101	69	4.225	1100000	96	4.900	
	0010000	16	2.900	0101011	43	3.575	1000110	70	4.250	1100001	97	4.925	
	0010001	17	2.925	0101100	44	3.600	1000111	71	4.275	1100010	98	4.950	
	0010010	18	2.950	0101101	45	3.625	1001000	72	4.300	1100011	99	4.975	
	0010011	19	2.975	0101110	46	3.650	1001001	73	4.325	1100100	100	5.000	
	0010100	20	3.000	0101111	47	3.675	1001010	74	4.350	1100101	101		
	0010101	21	3.025	0110000	48	3.700	1001011	75	4.375				Not Permitted
	0010110	22	3.050	0110001	49	3.725	1001100	76	4.400	0111111	127		
	0010111	23	3.075	0110010	50	3.750	1001101	77	4.425				
	0011000	24	3.100	0110011	51	3.775	1001110	78	4.450				
	0011001	25	3.125	0110100	52	3.800	1001111	79	4.475				
	0011010	26	3.150	0110101	53	3.825	1010000	80	4.500				
	-Set VCOML Voltage												
	VML[6:0]		VCOML	VML[6:0]	VCOML	VML[6:0]	VCOML	VML[6:0]	VCOML	VML[6:0]	VCOML		
	0000000	0	-2.500	0011011	27	-1.825	0110110	54	-1.150	1010001	81	-0.475	
	0000001	1	-2.475	0011100	28	-1.800	0110111	55	-1.125	1010010	82	-0.450	
	0000010	2	-2.450	0011101	29	-1.775	0111000	56	-1.100	1010011	83	-0.425	
	0000011	3	-2.425	0011110	30	-1.750	0111001	57	-1.075	1010100	84	-0.400	
	0000100	4	-2.400	0011111	31	-1.725	0111010	58	-1.050	1010101	85	-0.375	
	0000101	5	-2.375	0100000	32	-1.700	0111011	59	-1.025	1010110	86	-0.350	
	0000110	6	-2.350	0100001	33	-1.675	0111100	60	-1.000	1010111	87	-0.325	
	0000111	7	-2.325	0100010	34	-1.650	0111101	61	-0.975	1011000	88	-0.300	
	0001000	8	-2.300	0100011	35	-1.625	0111110	62	-0.950	1011001	89	-0.275	
	0001001	9	-2.275	0100100	36	-1.600	0111111	63	-0.925	1011010	90	-0.250	
	0001010	10	-2.250	0100101	37	-1.575	1000000	64	-0.900	1011011	91	-0.225	
	0001011	11	-2.225	0100110	38	-1.550	1000001	65	-0.875	1011100	92	-0.200	
	0001100	12	-2.200	0100111	39	-1.525	1000010	66	-0.850	1011101	93	-0.175	
	0001101	13	-2.175	0101000	40	-1.500	1000011	67	-0.825	1011110	94	-0.150	
	0001110	14	-2.150	0101001	41	-1.475	1000100	68	-0.800	1011111	95	-0.125	
	0001111	15	-2.125	0101010	42	-1.450	1000101	69	-0.775	1100000	96	-0.100	
	0010000	16	-2.100	0101011	43	-1.425	1000110	70	-0.750	1100001	97	-0.075	
	0010001	17	-2.075	0101100	44	-1.400	1000111	71	-0.725	1100010	98	-0.050	
	0010010	18	-2.050	0101101	45	-1.375	1001000	72	-0.700	1100011	99	-0.025	
	0010011	19	-2.025	0101110	46	-1.350	1001001	73	-0.675	1100100	100	0.000	
	0010100	20	-2.000	0101111	47	-1.325	1001010	74	-0.650	1100101	101		
	0010101	21	-1.975	0110000	48	-1.300	1001011	75	-0.625				Not Permitted
	0010110	22	-1.950	0110001	49	-1.275	1001100	76	-0.600	1111111	127		
	0010111	23	-1.925	0110010	50	-1.250	1001101	77	-0.575				
	0011000	24	-1.900	0110011	51	-1.225	1001110	78	-0.550				
	0011001	25	-1.875	0110100	52	-1.200	1001111	79	-0.525				
	0011010	26	-1.850	0110101	53	-1.175	1010000	80	-0.500				
Restriction	-If this register not using the register need be reserved. -The VCOM amplitude: VCOMH-VCOML <=5.5V -The deviation value of VCOMH/VCOML between with Measurement and Specification: Max <=25mV -The deviation value of VCOMAC between with Measurement and Specification: Max <= 50mV												

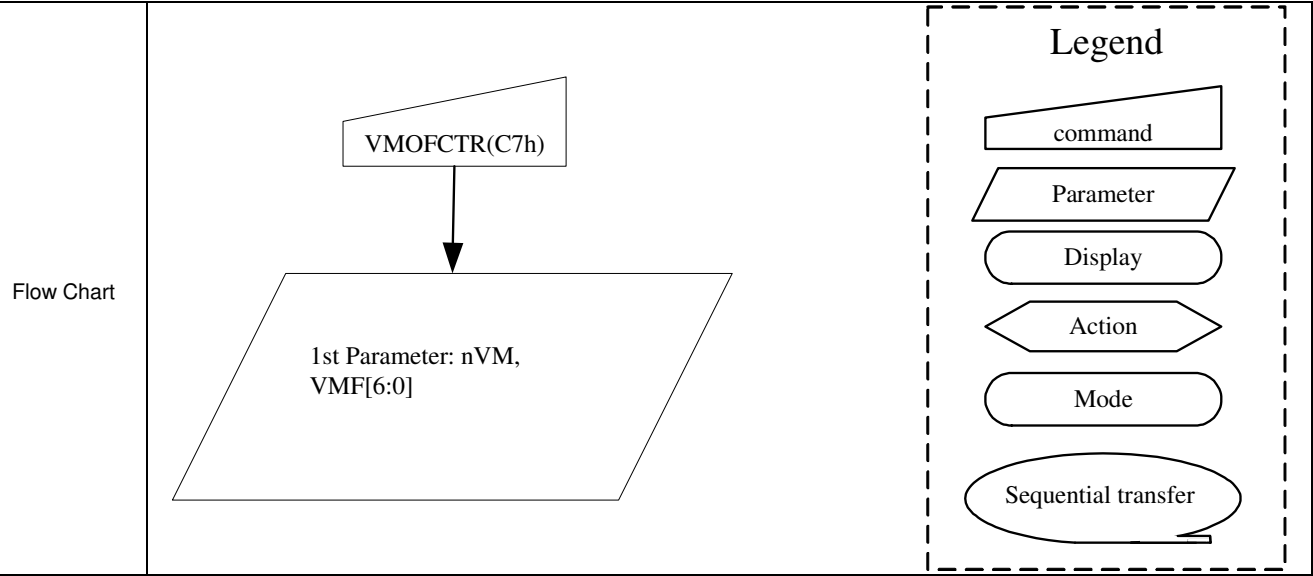
Register Availability	<table><tr><th colspan="2">Status</th><th colspan="2">Availability</th></tr><tr><td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td colspan="2">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td colspan="2">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td colspan="2">Sleep In</td><td colspan="2">Yes</td></tr></table>				Status		Availability		Normal Mode On, Idle Mode Off, Sleep Out		Yes		Normal Mode On, Idle Mode On, Sleep Out		Yes		Partial Mode On, Idle Mode Off, Sleep Out		Yes		Partial Mode On, Idle Mode On, Sleep Out		Yes		Sleep In		Yes	
	Status		Availability																									
	Normal Mode On, Idle Mode Off, Sleep Out		Yes																									
	Normal Mode On, Idle Mode On, Sleep Out		Yes																									
	Partial Mode On, Idle Mode Off, Sleep Out		Yes																									
	Partial Mode On, Idle Mode On, Sleep Out		Yes																									
Sleep In		Yes																										
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>nVM</th><th>VMH[6:0]</th><th>VML[6:0]</th></tr><tr><td>Power On Sequence</td><td>0d</td><td>67d</td><td>77d</td></tr><tr><td>SW Reset</td><td>0d</td><td>67d</td><td>77d</td></tr><tr><td>HW Reset</td><td>0d</td><td>67d</td><td>77d</td></tr></table>				Status	Default Value			nVM	VMH[6:0]	VML[6:0]	Power On Sequence	0d	67d	77d	SW Reset	0d	67d	77d	HW Reset	0d	67d	77d					
	Status	Default Value																										
		nVM	VMH[6:0]	VML[6:0]																								
	Power On Sequence	0d	67d	77d																								
	SW Reset	0d	67d	77d																								
HW Reset	0d	67d	77d																									
Flow Chart	<div><div>VMCTR(C5h)</div><div>↓</div><div>1st Parameter: VMH[6:0] 2nd Parameter: VML[6:0]</div></div>																											
	<div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																											

### 14.2.50 VCOM\_Control 2 (C6h)

C6H	VCOM_Control2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	1	1	0	0	0	1	1	0	C6h
1 <sup>st</sup> Parameter	1	1		x	0	0	VMA5	VMA4	VMA3	VMA2	VMA1	VMA0	13h/06h
Description	-Set VCOMAC Voltage In this case, these registers don't be used.												
Restriction	-												
Register Availability	-												
Default	-												

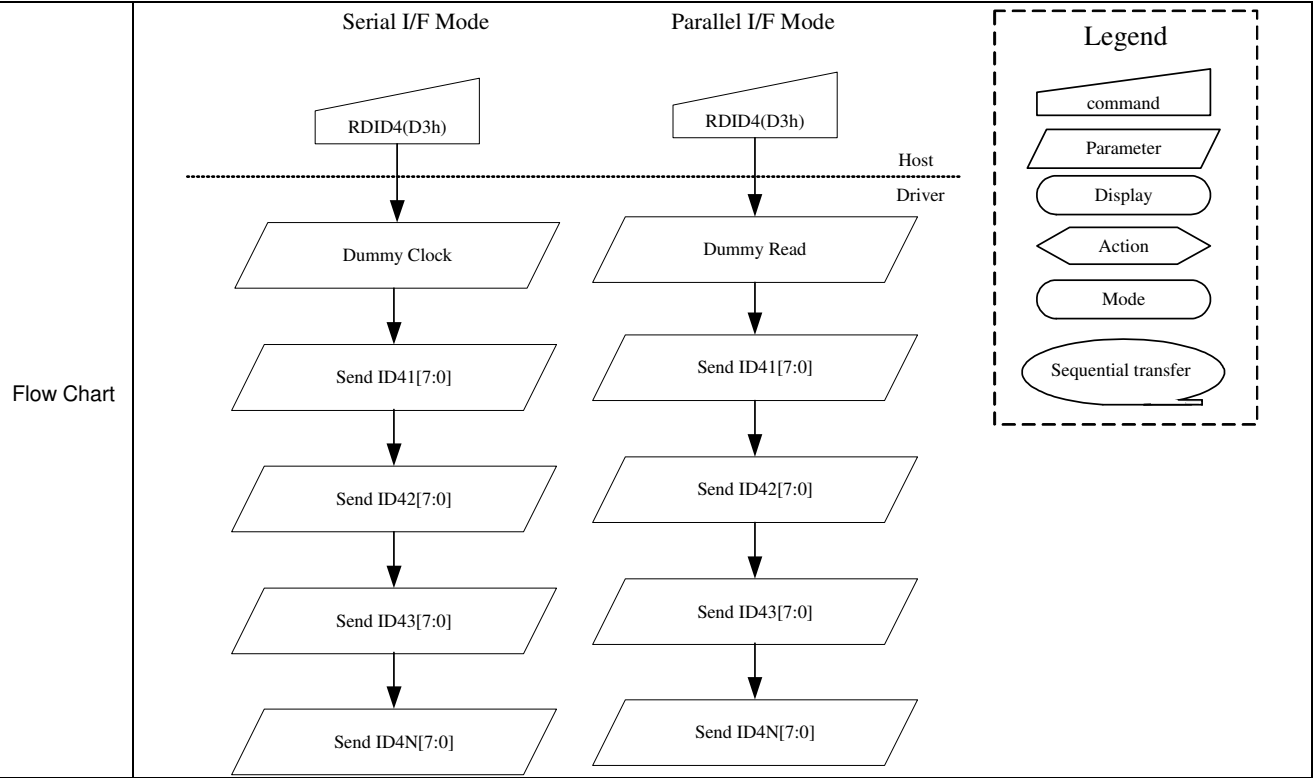
### 14.2.51 VCOM Offset Control (C7h)

C7H				VCOM Offset Control																																																
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1		x	1	1	0	0	0	1	1	1	C7h																																							
1 <sup>st</sup> Parameter	1	1		0	nVM*	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	40h																																							
Description	-Set VCOMH Voltage																																																			
	<table><tr><th>VMF[6:0]</th><th>VCOMH Output</th><th>VCOML Output Level</th></tr><tr><td>0</td><td>“VMH”</td><td>“VML”</td></tr><tr><td>1</td><td>“VMH”-63d</td><td>“VML”-63d</td></tr><tr><td>2</td><td>“VMH”-62d</td><td>“VML”-62d</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>62</td><td>“VMH”-2d</td><td>“VML”-2d</td></tr><tr><td>63</td><td>“VMH”-1d</td><td>“VML”-1d</td></tr><tr><td>64</td><td>“VMH”</td><td>“VML”</td></tr><tr><td>65</td><td>“VMH”+1d</td><td>“VML”+1d</td></tr><tr><td>66</td><td>“VMH”+2d</td><td>“VML”+2d</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>126</td><td>“VMH”+62d</td><td>“VML”+62d</td></tr><tr><td>127</td><td>“VMH”+63d</td><td>“VML”+63d</td></tr></table>													VMF[6:0]	VCOMH Output	VCOML Output Level	0	“VMH”	“VML”	1	“VMH”-63d	“VML”-63d	2	“VMH”-62d	“VML”-62d	:	:	:	62	“VMH”-2d	“VML”-2d	63	“VMH”-1d	“VML”-1d	64	“VMH”	“VML”	65	“VMH”+1d	“VML”+1d	66	“VMH”+2d	“VML”+2d	:	:	:	126	“VMH”+62d	“VML”+62d	127	“VMH”+63d	“VML”+63d
	VMF[6:0]	VCOMH Output	VCOML Output Level																																																	
	0	“VMH”	“VML”																																																	
	1	“VMH”-63d	“VML”-63d																																																	
	2	“VMH”-62d	“VML”-62d																																																	
	:	:	:																																																	
	62	“VMH”-2d	“VML”-2d																																																	
	63	“VMH”-1d	“VML”-1d																																																	
	64	“VMH”	“VML”																																																	
	65	“VMH”+1d	“VML”+1d																																																	
	66	“VMH”+2d	“VML”+2d																																																	
	:	:	:																																																	
	126	“VMH”+62d	“VML”+62d																																																	
	127	“VMH”+63d	“VML”+63d																																																	
	If “VMH”+xd or “VML”+xd is less than 0d, it becomes 0d																																																			
	If “VMH”+xd or “VML”+xd is large than 100d, it becomes 100d																																																			
	VMF[5:0] are stored in NV memory to contrast																																																			
-Select the VMF[6:0]value																																																				
<table><tr><td>nVM</td><td>VMF[6:0] value</td></tr><tr><td>0</td><td>VCOM offset value from NV memory</td></tr><tr><td>1</td><td>VCOM offset value in the VMF[6:0] registers</td></tr></table>													nVM	VMF[6:0] value	0	VCOM offset value from NV memory	1	VCOM offset value in the VMF[6:0] registers																																		
nVM	VMF[6:0] value																																																			
0	VCOM offset value from NV memory																																																			
1	VCOM offset value in the VMF[6:0] registers																																																			
Restriction	-If this register not use the register need be reserved. -To control the VCOM output voltage with VMF[5::0] command, nVM parameter should be set ‘1’																																																			
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																											
Status	Availability																																																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																			
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																																			
Partial Mode On, Idle Mode On, Sleep Out	Yes																																																			
Sleep In	Yes																																																			
Default	<table><tr><th>Status</th><th>Default Value VMF[6:0]</th></tr><tr><td>Power On Sequence</td><td>40h</td></tr><tr><td>SW Reset</td><td>40h</td></tr><tr><td>HW Reset</td><td>40h</td></tr></table>													Status	Default Value VMF[6:0]	Power On Sequence	40h	SW Reset	40h	HW Reset	40h																															
Status	Default Value VMF[6:0]																																																			
Power On Sequence	40h																																																			
SW Reset	40h																																																			
HW Reset	40h																																																			



## 14.2.52 Write ID4 Value (D3h)

D3H	Read the ID4 value																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1		x	1	1	0	1	0	0	1	1	D3h																			
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x																			
2 <sup>nd</sup> Parameter	1		1	x	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	91h																			
3 <sup>rd</sup> Parameter	1		1	x	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	63h																			
4 <sup>th</sup> Parameter	1		1	x	x	x	x	x	ID433	ID432	ID431	ID430	00h																			
5 <sup>th</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x																			
Description	<div>-Read the Driver IC information from mask value.</div> <div>-Ignored the EXTC pin.</div> <div>-The 1<sup>st</sup> parameter is dummy data</div> <div>-The 2<sup>nd</sup> parameter ID41[7:0] is Driver IC ID code. (Default value=91h)</div> <div>-The value be defined later</div> <div>-Currently, “01h”, “02h”, “03h”, “05h” can’t be used.</div> <div>-The 3<sup>rd</sup> parameter ID42[7:0] is Driver IC Part number ID. (The code be define by Driver IC Vendor, and default value=63h)</div> <div>-The 4<sup>th</sup> parameter ID43[7:0] is Driver IC version ID</div> <div>-When the Driver maker modifies any function it should be modify the parameters at this ID code before sample out also.</div> <div>-If Driver Maker don’t need 2 parameter if can’t reduce to one parameter.</div> <div>-If the parameters are not enough Driver makers can add or reduce yourself</div>																															
Restriction	-																															
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In	Yes																															
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>ID41[7:0]</th><th>ID42[7:0]</th><th>ID43[7:0]</th></tr><tr><td>Power On Sequence</td><td>01h</td><td>21h</td><td>TBD</td></tr><tr><td>SW Reset</td><td>01h</td><td>21h</td><td>TBD</td></tr><tr><td>HW Reset</td><td>01h</td><td>21h</td><td>TBD</td></tr></table>													Status	Default Value			ID41[7:0]	ID42[7:0]	ID43[7:0]	Power On Sequence	01h	21h	TBD	SW Reset	01h	21h	TBD	HW Reset	01h	21h	TBD
Status	Default Value																															
	ID41[7:0]	ID42[7:0]	ID43[7:0]																													
Power On Sequence	01h	21h	TBD																													
SW Reset	01h	21h	TBD																													
HW Reset	01h	21h	TBD																													



### 14.2.53 NV Memory Function Controller(1) (D5h)

D5H	NV Memory Function Controller1																																																																	
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																					
Command	0	1		x	1	1	0	1	1	0	1	0	D5h																																																					
1 <sup>st</sup> Parameter	1	1		x	ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20	00h																																																					
2 <sup>nd</sup> Parameter	1	1		x	OTP_ BS	0	0	0	OTP_ VMF3	OTP_ VMF2	OTP_ VMF1	OTP_ VMF0	00h																																																					
Description	-ID2,ID3,and VMF can be written four times.																																																																	
	-Read status(written times) of the NV memory.																																																																	
	-Written times for ID2																																																																	
	<table><tr><th rowspan="2">Times \ ID2</th><th colspan="8">1<sup>st</sup> Parameter</th></tr><tr><th>ID33</th><th>ID32</th><th>ID31</th><th>ID30</th><th>ID23</th><th>ID22</th><th>ID21</th><th>ID20</th></tr><tr><td>1<sup>st</sup></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>2<sup>nd</sup></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>3<sup>rd</sup></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>4<sup>th</sup></td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>													Times \ ID2	1 <sup>st</sup> Parameter								ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20	1 <sup>st</sup>	0	0	0	0	0	0	0	1	2 <sup>nd</sup>	0	0	0	0	0	0	1	1	3 <sup>rd</sup>	0	0	0	0	0	1	1	1	4 <sup>th</sup>	0	0	0	0	1	1	1	1
	Times \ ID2	1 <sup>st</sup> Parameter																																																																
ID33		ID32	ID31	ID30	ID23	ID22	ID21	ID20																																																										
1 <sup>st</sup>	0	0	0	0	0	0	0	1																																																										
2 <sup>nd</sup>	0	0	0	0	0	0	1	1																																																										
3 <sup>rd</sup>	0	0	0	0	0	1	1	1																																																										
4 <sup>th</sup>	0	0	0	0	1	1	1	1																																																										
	-Written times for ID3																																																																	
	<table><tr><th rowspan="2">Times \ ID3</th><th colspan="8">1<sup>st</sup> Parameter</th></tr><tr><th>ID33</th><th>ID32</th><th>ID31</th><th>ID30</th><th>ID23</th><th>ID22</th><th>ID21</th><th>ID20</th></tr><tr><td>1<sup>st</sup></td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>2<sup>nd</sup></td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>3<sup>rd</sup></td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>4<sup>th</sup></td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>													Times \ ID3	1 <sup>st</sup> Parameter								ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20	1 <sup>st</sup>	0	0	0	1	0	0	0	0	2 <sup>nd</sup>	0	0	1	1	0	0	0	0	3 <sup>rd</sup>	0	1	1	1	0	0	0	0	4 <sup>th</sup>	1	1	1	1	0	0	0	0
Times \ ID3	1 <sup>st</sup> Parameter																																																																	
	ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20																																																										
1 <sup>st</sup>	0	0	0	1	0	0	0	0																																																										
2 <sup>nd</sup>	0	0	1	1	0	0	0	0																																																										
3 <sup>rd</sup>	0	1	1	1	0	0	0	0																																																										
4 <sup>th</sup>	1	1	1	1	0	0	0	0																																																										
	-Written times for OTP_VMF																																																																	



## 14.2.54 NV Memory Function Controller(2) (D6h)

D6H	NV Memory Function Controller1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		x	1	1	0	1	1	0	1	0	D6h
1 <sup>st</sup> Parameter	1	1		x	OTP_ D[7]	OTP_ D[6]	OTP_ D[5]	OTP_ D[4]	OTP_ D[3]	OTP_ D[2]	OTP_ D[1]	OTP_ D[0]	00h
2 <sup>nd</sup> Parameter	1	1		x	0	0	0	0	0	0	OTP_ TP[1]	OTP_ TP[0]	00h
Description	-Parameter 1												
	bit[7:0] :      OTP Write Data                  OTP_D[7:0]												
	ID2[7:0]												
	ID3[7:0]												
	{1'b0, VMF[6:0]}												
	Ctrl[4:0] -> {3'd0, BG_AD[1:0], OSC_CT[2:0]}												
Description	-Parameter 2      OTP type selection:												
	bit[1:0] :      OTP Address                  OTP[1:0]												
	00: ID2,      01:ID3,      10:VMF,      11:Ctrl												
	MTP write EPWRITE command												
	Please see MTP Access sequence for program(Data write) for more detail												
Register Availability													
Default													
Flow Chart													

### 14.2.55 NV Memory Function Controller(3) (D7h)

D7H	NV Memory Function Controller1																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	1	1	0	1	1	0	1	0	D7h												
1 <sup>st</sup> Parameter	1	1		x	0	1	0	1	0	1	0	1	55h												
2 <sup>nd</sup> Parameter	1	1		x	1	0	1	0	1	0	1	0	AAh												
3 <sup>rd</sup> Parameter	1	1		x	0	1	1	0	0	1	1	0	66h												
Description	MTP write EPWRITE command Please see MTP Access sequence for program(Data write) for more detail																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart																									

### 14.2.34 Read ID1 (DAh)

DAH	RDID1 (Read ID1)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	1	1	0	1	1	0	1	0	DAh												
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x												
2 <sup>nd</sup> Parameter	1		1	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	54h												
Description	<p>This read byte return 8-bit LCD module's ID.</p> <p>The 1<sup>st</sup> parameter is dummy data</p> <p>The 2<sup>nd</sup> parameter (ID17to ID10): LCD module manufacturer ID</p> <p>X = Don't care</p>																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>54h</td></tr><tr><td>SW Reset</td><td>54h</td></tr><tr><td>HW Reset</td><td>54h</td></tr></table> <p>Note : ID1 can be modified by metal option</p>													Status	Default Value	Power On Sequence	54h	SW Reset	54h	HW Reset	54h				
Status	Default Value																								
Power On Sequence	54h																								
SW Reset	54h																								
HW Reset	54h																								
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDID1(DAh)</div><div>↓</div><div>Send 2nd parameter ID1[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDID1(DAh)</div><div>↓</div><div>Dummy Read</div><div>↓</div><div>Send 2nd parameter ID1[7:0]</div></div></div><div><div>Host</div><div>Driver</div></div></div> <div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

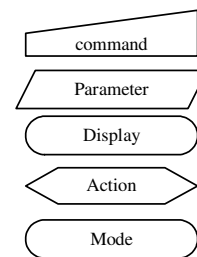
### 14.2.35 Read ID2 (DBh)

DBH	RDID2 (Read ID2)																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1		x	1	1	0	1	1	0	1	1	DBh																		
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x																		
2 <sup>nd</sup> Parameter	1		1	x	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h																		
Description	<p>This read byte returns 8-bit LCD module/driver version ID</p> <p>Th<sup>o</sup> 1st parameter is dummy data</p> <p>Th<sup>o</sup> 2nd parameter (ID26 to ID20): LCD module/driver version ID</p> <p>Parameter Range: ID=80h to FFh</p> <p>Note : See command RDDID(04h) 3rd parameter</p> <table><tr><th>D7 to D0</th><th>Version</th><th>Changes</th></tr><tr><td>80h</td><td>TBD</td><td>TBD</td></tr><tr><td>81h</td><td>TBD</td><td>TBD</td></tr><tr><td>82h</td><td>TBD</td><td>TBD</td></tr><tr><td>83h</td><td>TBD</td><td>TBD</td></tr><tr><td>-</td><td>TBD</td><td>TBD</td></tr></table>													D7 to D0	Version	Changes	80h	TBD	TBD	81h	TBD	TBD	82h	TBD	TBD	83h	TBD	TBD	-	TBD	TBD
D7 to D0	Version	Changes																													
80h	TBD	TBD																													
81h	TBD	TBD																													
82h	TBD	TBD																													
83h	TBD	TBD																													
-	TBD	TBD																													
Restriction																															
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
Partial Mode On, Idle Mode Off, Sleep Out	Yes																														
Partial Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In	Yes																														
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>See Description</td></tr><tr><td>SW Reset</td><td>See Description</td></tr><tr><td>HW Reset</td><td>See Description</td></tr></table>													Status	Default Value	Power On Sequence	See Description	SW Reset	See Description	HW Reset	See Description										
Status	Default Value																														
Power On Sequence	See Description																														
SW Reset	See Description																														
HW Reset	See Description																														
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDID2(DBh)</div><div>↓</div><div>Send 2nd parameter ID2[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDID2(DBh)</div><div>↓</div><div>Dummy Read</div><div>↓</div><div>Send 2nd parameter ID2[7:0]</div></div></div><div><div>Host</div><div>Driver</div></div></div> <div><div>Legend</div><div><div>command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																														

### 14.2.36 Read ID3 (DCh)

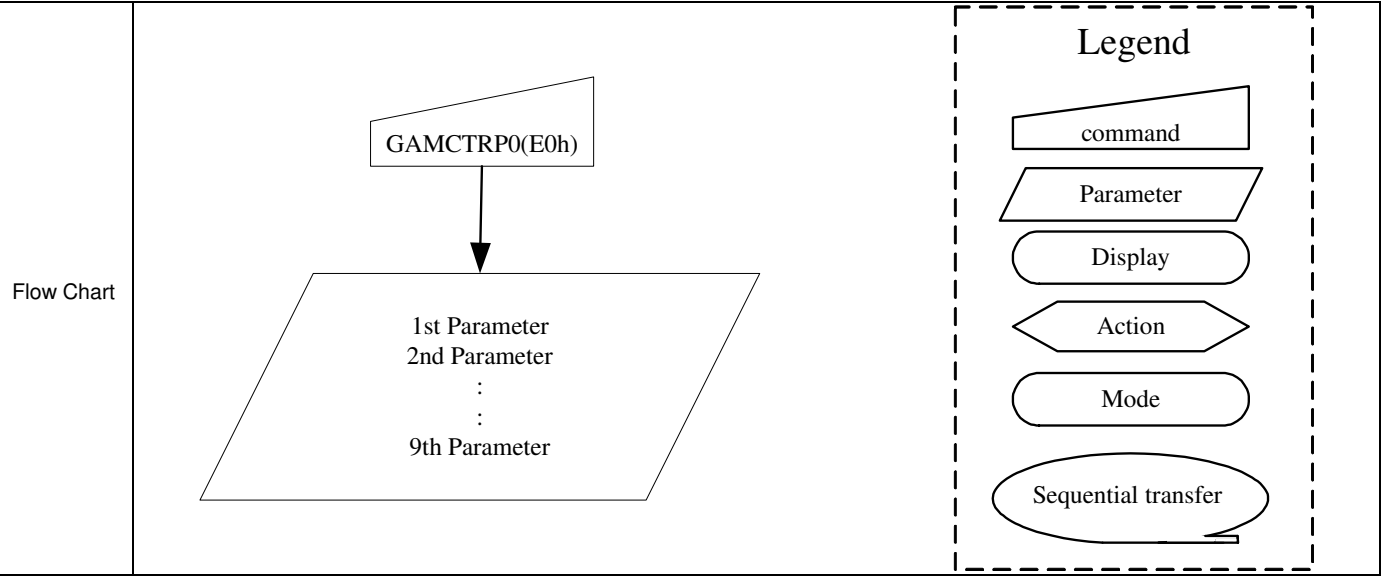
DCH	RDID3 (Read ID3)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		x	1	1	0	1	1	1	0	0	DCh												
1 <sup>st</sup> Parameter	1		1	x	x	x	x	x	x	x	x	x	x												
2 <sup>nd</sup> Parameter	1		1	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	66h												
Description	<div>-This read byte return 8-bit LCD module/driver ID</div> <div>-Th<sup>e</sup> 1st parameter is dummy data</div> <div>-Th<sup>e</sup> 2nd parameter (ID37 to ID30): LCD module/driver ID</div> <div>-Parameter range: ID=00h to FFh</div> <div>Note : See command RDDID(04h) 4th parameter</div>																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>66h</td></tr><tr><td>SW Reset</td><td>66h</td></tr><tr><td>HW Reset</td><td>66h</td></tr></table>													Status	Default Value	Power On Sequence	66h	SW Reset	66h	HW Reset	66h				
Status	Default Value																								
Power On Sequence	66h																								
SW Reset	66h																								
HW Reset	66h																								

Flow Chart



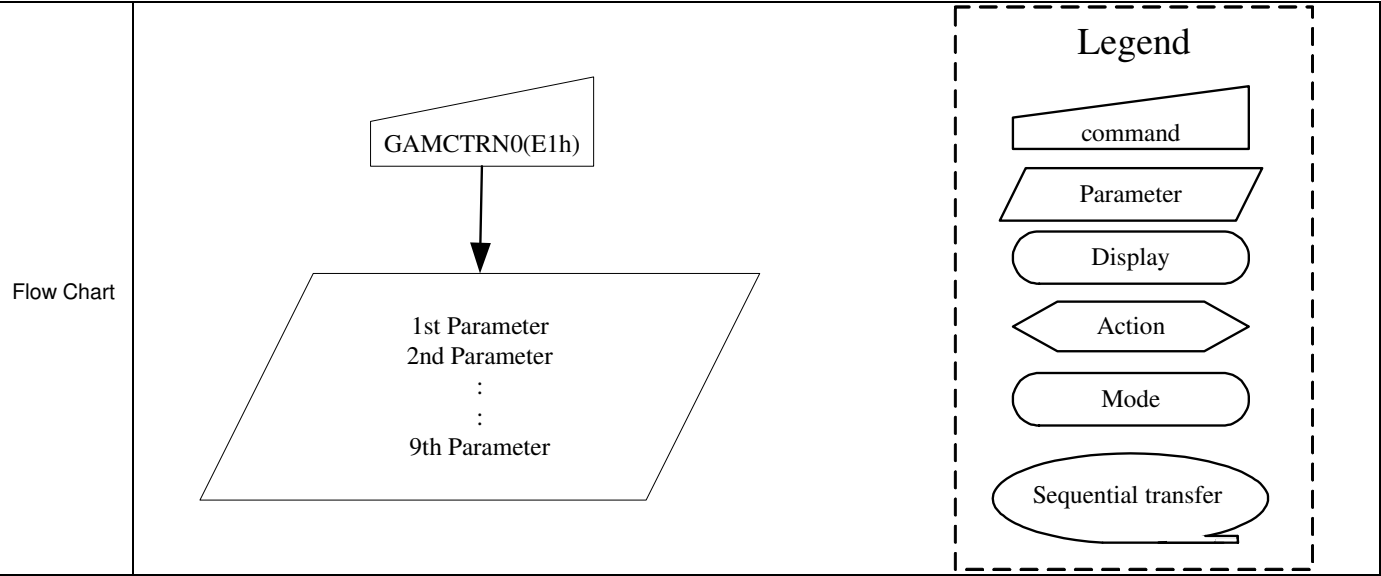
## 14.2.56 Positive Gamma Correction Setting (E0h)

E1H	Postive Gamma Correction Setting																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		1	1	1	0	0	0	0	1	E1h												
1 <sup>st</sup> Parameter	1	1		x	x	VP0[5:0]						x												
2 <sup>nd</sup> Parameter	1	1		x	x	VP1[5:0]						x												
3 <sup>rd</sup> Parameter	1	1		x	x	VP2[5:0]						x												
4 <sup>th</sup> Parameter	1	1		x	x	VP4[5:0]						x												
5 <sup>th</sup> Parameter	1	1		x	x	VP6[5:0]						x												
6 <sup>th</sup> Parameter	1	1		x	x	x	VP13[4:0]					x												
7 <sup>th</sup> Parameter	1	1		x	VP20[6:0]							x												
8 <sup>th</sup> Parameter	1	1		VP36[3:0]				VP27[3:0]				x												
9 <sup>th</sup> Parameter	1	1		x	VP43[6:0]							x												
10 <sup>th</sup> Parameter	1	1		x	x	x	VP50[4:0]					x												
11 <sup>th</sup> Parameter	1	1		x	x	VP57[5:0]						x												
12 <sup>th</sup> Parameter	1	1		x	x	VP59[5:0]						x												
13 <sup>th</sup> Parameter	1	1		x	x	VP61[5:0]						x												
14 <sup>th</sup> Parameter	1	1		x	x	VP62[5:0]						x												
15 <sup>th</sup> Parameter	1	1		x	x	VP63[5:0]						x												
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. It apply to gamma curve selection for only activate when EXTC=1 and GAM_R_SEL=1																							
Restriction	-																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td></td><td>1<sup>st</sup> ~ 9<sup>th</sup> Parameter</td></tr><tr><td>Power On Sequence</td><td>All "00"</td></tr><tr><td>SW Reset</td><td>All "00"</td></tr><tr><td>HW Reset</td><td>All "00"</td></tr></table>												Status	Default Value		1 <sup>st</sup> ~ 9 <sup>th</sup> Parameter	Power On Sequence	All "00"	SW Reset	All "00"	HW Reset	All "00"		
Status	Default Value																							
	1 <sup>st</sup> ~ 9 <sup>th</sup> Parameter																							
Power On Sequence	All "00"																							
SW Reset	All "00"																							
HW Reset	All "00"																							



### 14.2.57 Negative Gamma Correction Setting (E1h)

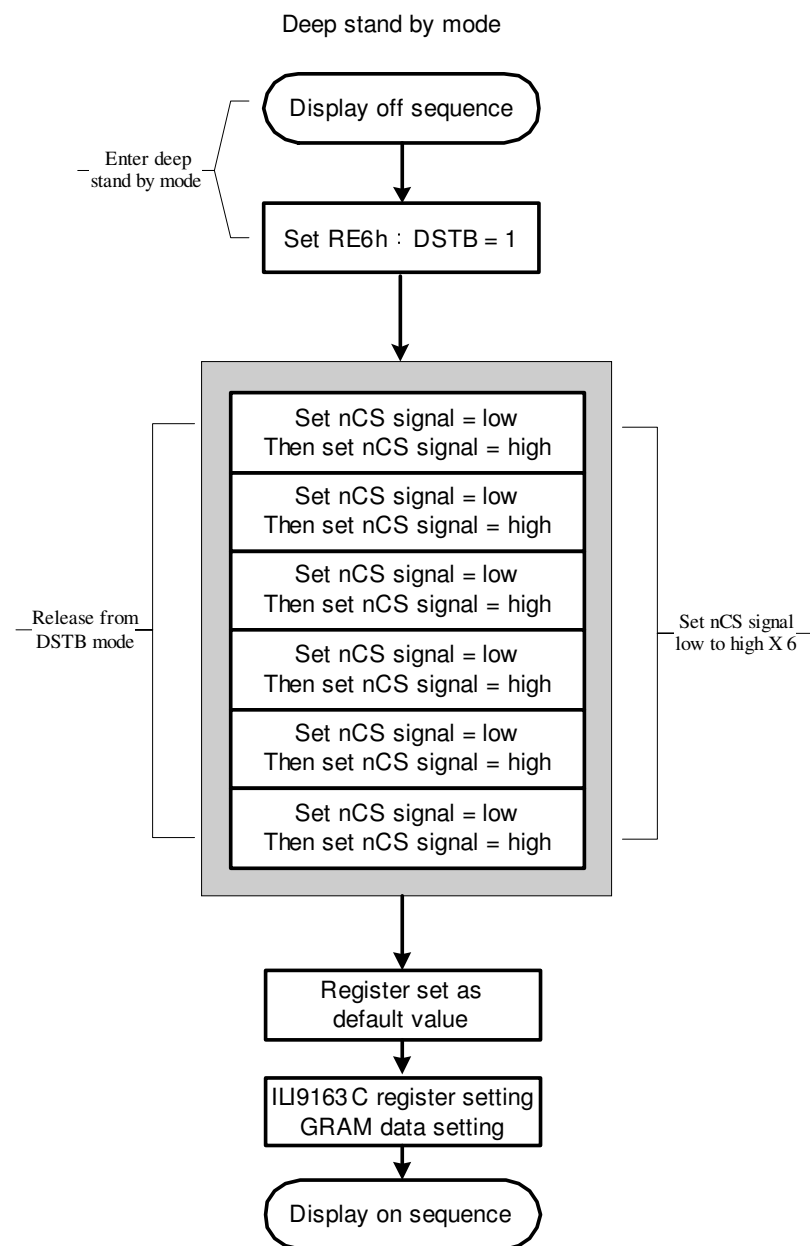
E1H	Negative Gamma Correction Setting																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		1	1	1	0	0	0	0	1	E1h												
1 <sup>st</sup> Parameter	1	1		x	x	VN63[5:0]						x												
2 <sup>nd</sup> Parameter	1	1		x	x	VN62[5:0]						x												
3 <sup>rd</sup> Parameter	1	1		x	x	VN61[5:0]						x												
4 <sup>th</sup> Parameter	1	1		x	x	VN59[5:0]						x												
5 <sup>th</sup> Parameter	1	1		x	x	VN57[5:0]						x												
6 <sup>th</sup> Parameter	1	1		x	x	x	VN50[4:0]					x												
7 <sup>th</sup> Parameter	1	1		x	VN43[6:0]						x													
8 <sup>th</sup> Parameter	1	1		VN27[3:0]				VN36[3:0]				x												
9 <sup>th</sup> Parameter	1	1		x	VN20[6:0]						x													
10 <sup>th</sup> Parameter	1	1		x	x	x	VN13[4:0]					x												
11 <sup>th</sup> Parameter	1	1		x	x	VN6[5:0]						x												
12 <sup>th</sup> Parameter	1	1		x	x	VN4[5:0]						x												
13 <sup>th</sup> Parameter	1	1		x	x	VN2[5:0]						x												
14 <sup>th</sup> Parameter	1	1		x	x	VN1[5:0]						x												
15 <sup>th</sup> Parameter	1	1		x	x	VN0[5:0]						x												
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. It apply to gamma curve selection for only activate when EXTC=1 and GAM_R_SEL=1																							
Restriction	-																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td></td><td>1<sup>st</sup> ~ 9<sup>th</sup> Parameter</td></tr><tr><td>Power On Sequence</td><td>All "00"</td></tr><tr><td>SW Reset</td><td>All "00"</td></tr><tr><td>HW Reset</td><td>All "00"</td></tr></table>												Status	Default Value		1 <sup>st</sup> ~ 9 <sup>th</sup> Parameter	Power On Sequence	All "00"	SW Reset	All "00"	HW Reset	All "00"		
Status	Default Value																							
	1 <sup>st</sup> ~ 9 <sup>th</sup> Parameter																							
Power On Sequence	All "00"																							
SW Reset	All "00"																							
HW Reset	All "00"																							



14.2.58 Deep stand by control (E6h)

E6h	Deep stand by control											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		1	1	1	0	0	1	1	0	E6h
1 <sup>st</sup> Parameter	1	1		x	x	x	x	x	x	x	DSTB	x
Description	<p>When DSTB = 1, the ILI9163C enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the ILI9163C enters the deep standby mode, and they must be reset after exiting deep standby mode.</p> <p><b>1. Basic operation</b></p> <p>The basic operation modes of 9163C are as shown in the following diagram.</p> <pre>graph TD; DO[Display On] &lt;--&gt; DOff[Display Off]; DOff -- DSTBY --&gt; DS[Deep Standby]; DS -- Exit --&gt; R[Reset]; R -- Initial --&gt; DOff; RESET --&gt; R;</pre>											

## 2. CPU interface transition setting sequences



Restriction

-

Register  
Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0h
SW Reset	0h
HW Reset	0h

### 14.2.59 GAM\_R\_SEL (F2h)

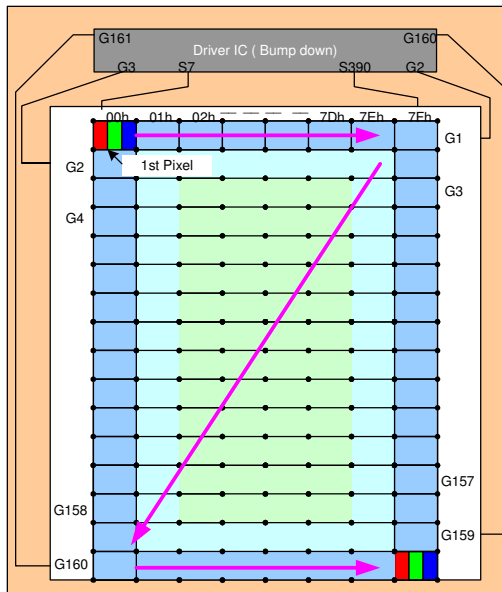
F2h	Gamma Setting (Green)																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1		1	1	1	1	0	0	1	0	F2h												
1 <sup>st</sup> Parameter	1	1		x	x	x	x	x	x	x	GAM_R_SEL	x												
Description	GAM_R_SEL: Gamma adjustment E0h and E1h enable control 0: Disable (Default) 1: Enable																							
Restriction	-																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0h</td></tr><tr><td>SW Reset</td><td>0h</td></tr><tr><td>HW Reset</td><td>0h</td></tr></table>												Status	Default Value	Power On Sequence	0h	SW Reset	0h	HW Reset	0h				
Status	Default Value																							
Power On Sequence	0h																							
SW Reset	0h																							
HW Reset	0h																							

## 15. Example Connection with Panel direction and Different Resolution

### 15.1 Application of connect with panel direction (when GM='011')

#### Case 1: (This is default case)

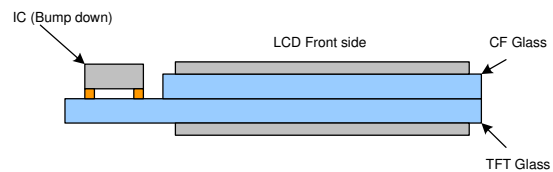
- 1<sup>st</sup> Pixel is at Left Top of the panle
- RGB filter order = RGB



- Direction default setting(H/W)  
SMX = 0  
SMY = 0  
SRGB = 0

S1 = Filter R  
S2 = Filter G  
S3 = Filter B

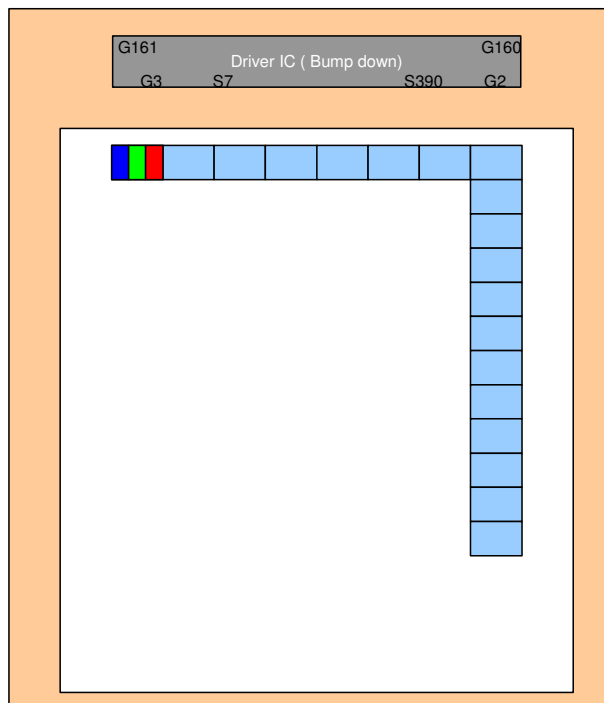
- Display direction control (S/W)  
- X- Mirror control by MX  
- Y- Mirror control by MY  
-XY- Exchange control by MV





Case 4:

- 1<sup>st</sup> Pixel is at Right-Bottom of the panel
- RGB filter order = "BGR"

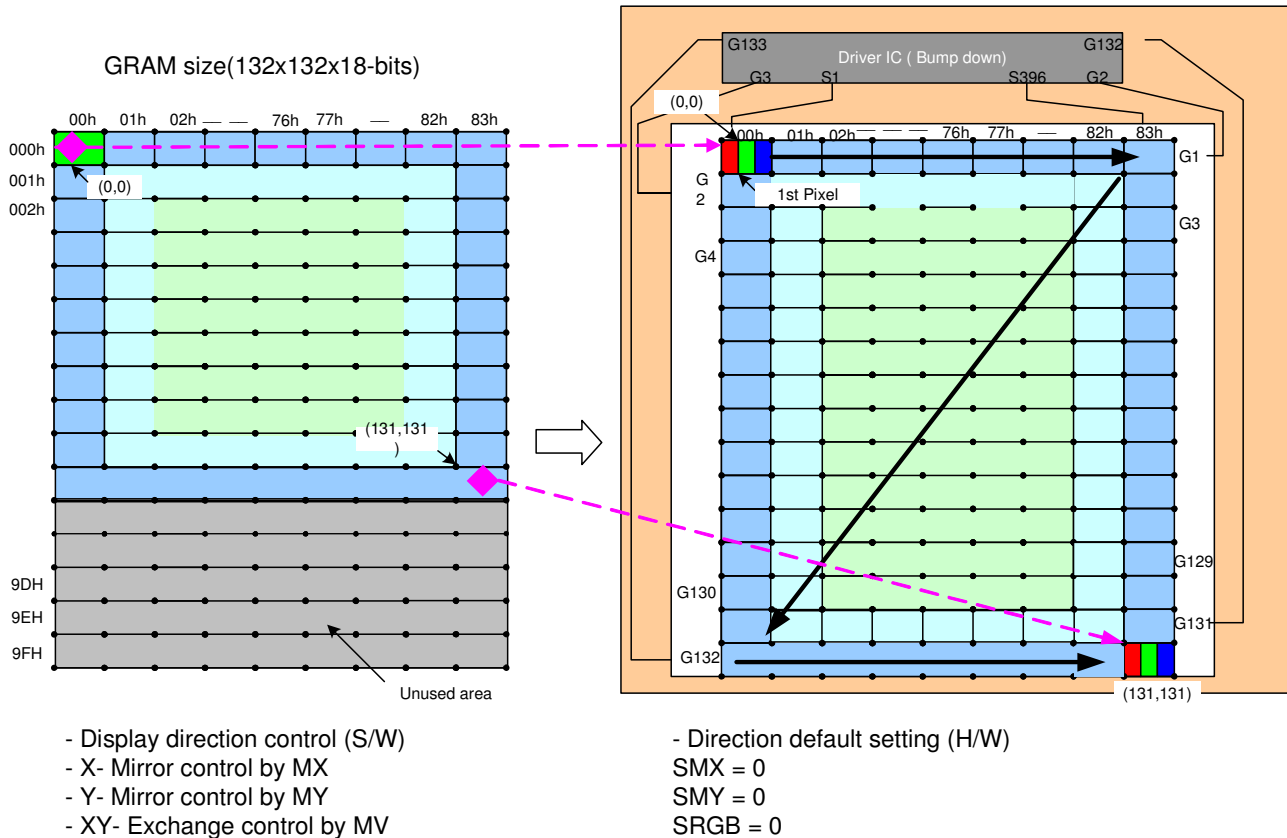


## 15.2 Application of connection with Different resolution

Case 1 of Resolution (132RGB x 132)(GM[2:0]="101") RAM size=132 x 132 x 18-bits(Used)

Display size = 132RGB x 132

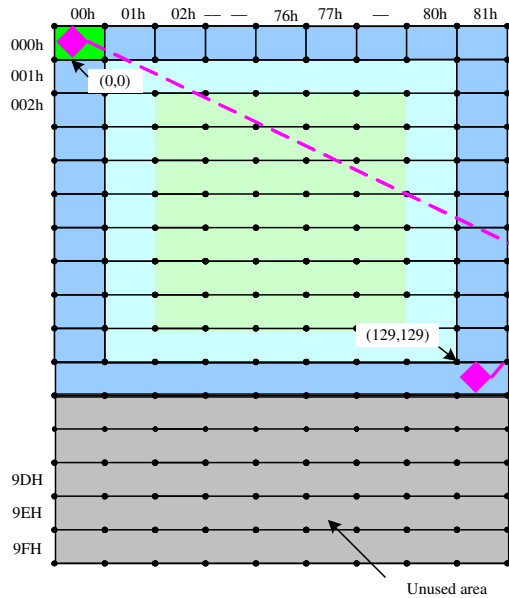
1) Example for SMX=SMY='0'



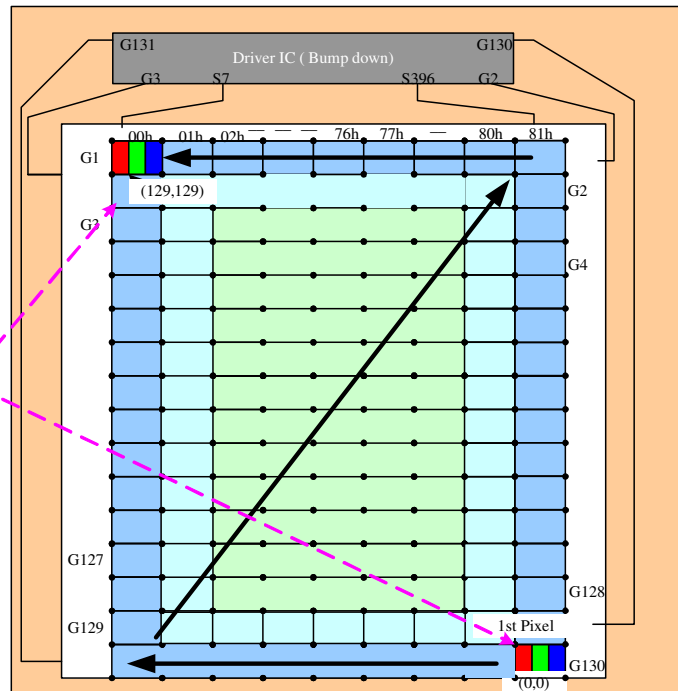


2) Example for SMX=SMY='1'

GRAM size(130x130x18-bits)



- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV



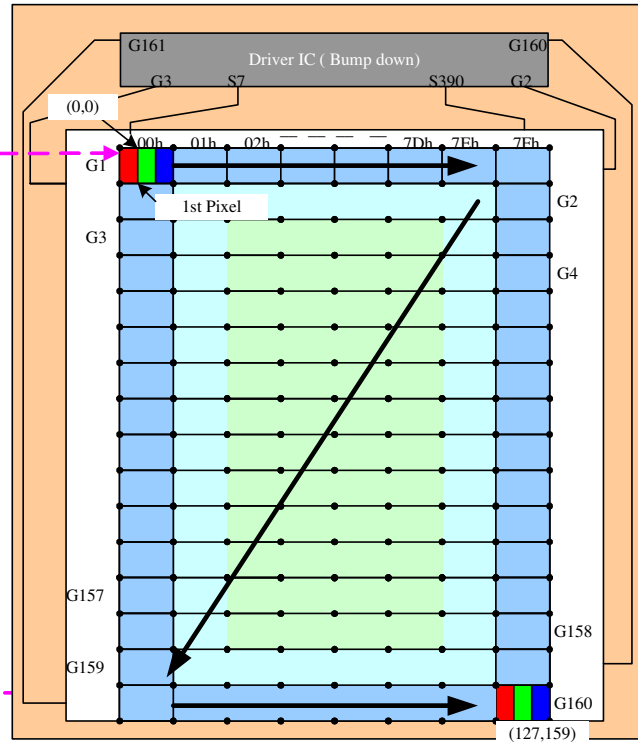
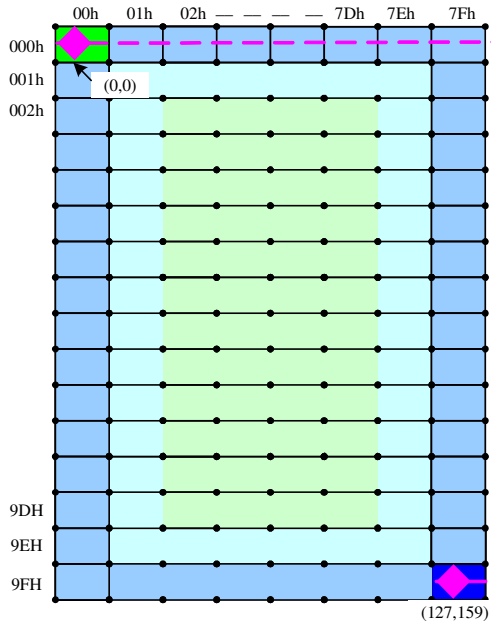
- Direction default setting (H/W)
- SMX = 1
- SMY = 1
- SRGB = 0

Case 3 of Resolution (128RGB x 160)(GM[2:0]="011") RAM size=128 x 160 x 18-bits(Used)

Display size = 128RGB x 160

1) Example for SMX=SMY='0'

GRAM size(128x160x18-bits)

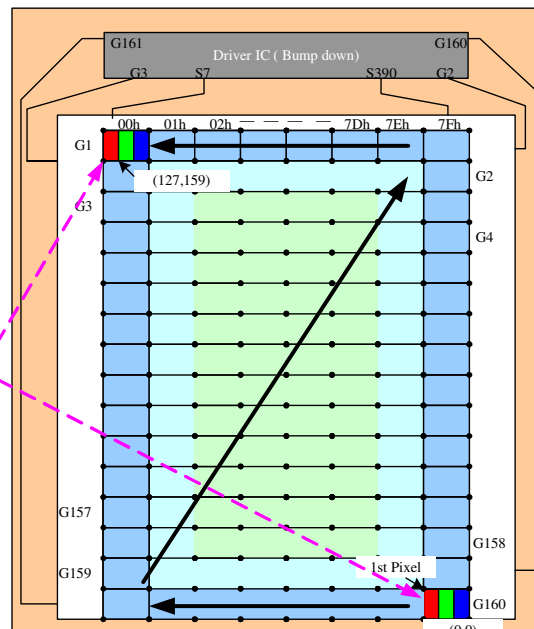
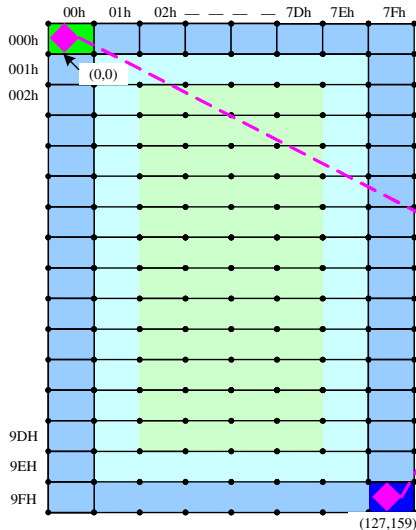


- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
- SMX = 0
- SMY = 0
- SRGB = 0

## 2) Example for SMX=SMY='1'

GRAM size(128x160x18-bits)



- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
- SMX = 1
- SMY = 1
- SRGB = 0

Case4 of Resolution (120RGB x 160)(GM[2:0]="010") RAM size=120 x 160 x 18-bits(Used)

Display size = 120RGB x 160

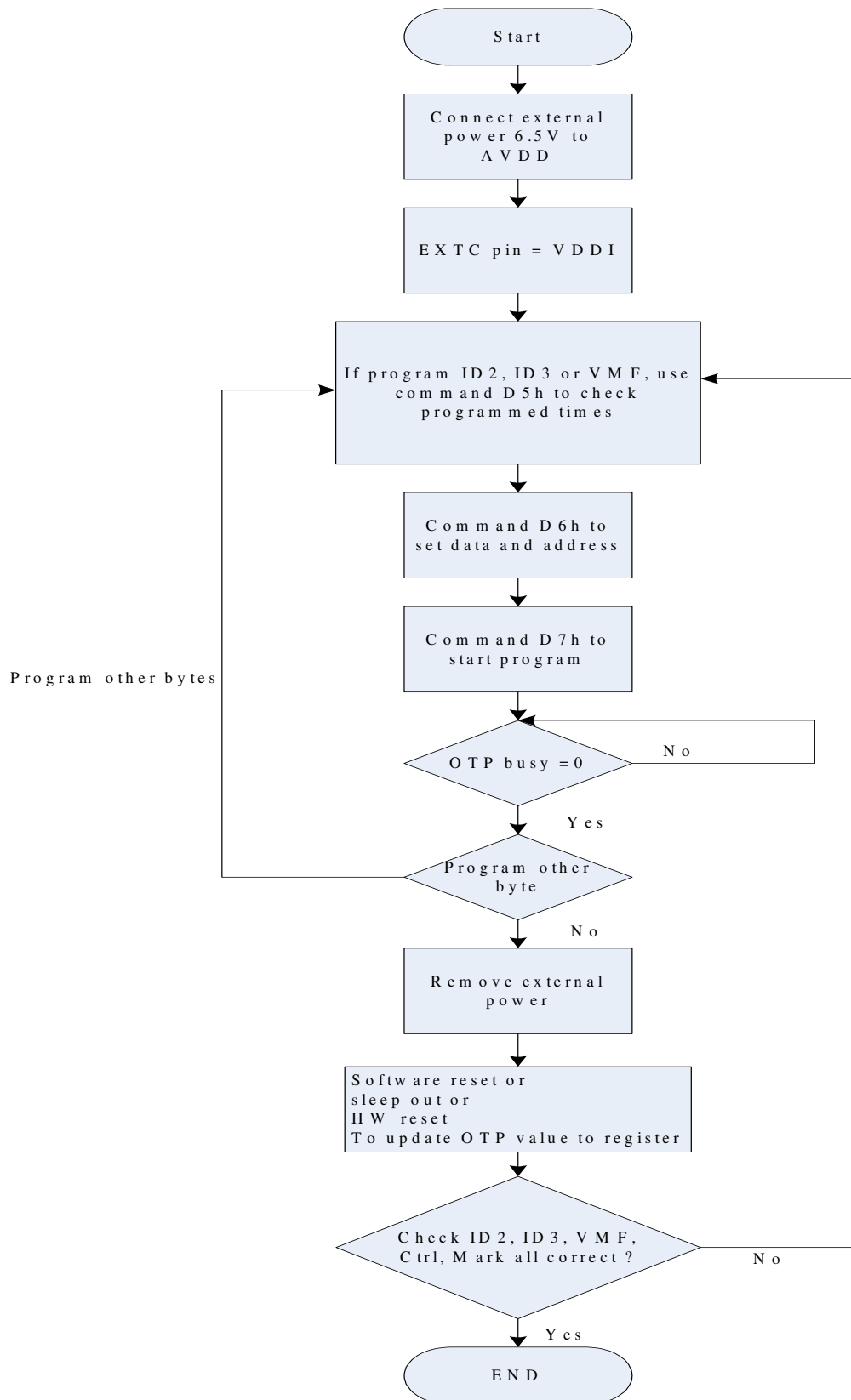
## 1) Example for SMX=SMY='0'







## 16. OTP Programming Flow



Note. Please remove external power 6.5V after programming.

## 17. Electrical Characteristics

### 17.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9163C is used out of the absolute maximum ratings, the ILI9163C may be permanently damaged. To use the ILI9163C within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9163C will malfunction and cause poor reliability.

Item	Symbol	Unit	Value Note
Supply voltage	VPNL	V	-0.3 ~ + 4.8
Supply voltage (Logic)	VDDI	V	-0.3 ~ + 4.6
Supply voltage (Digital)	VCC	V	-0.3 ~ + 2.4
Driver supply voltage	VGH-VGL	V	-0.3 ~ + 33.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	°C	-40 ~ + 85
Storage temperature	Tstg	°C	-55 ~ + 110

Notes: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

### 17.2 DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
<b>Power &amp; Operation Voltage</b>							
Analog Operating voltage	VPNL	V	Operating voltage	2.5	2.78	4.8	Note2
Logic Operating voltage	VDDI	V	I/O supply voltage	1.65	1.8/2.78	3.3	Note2
Digital Operating voltage	VCC	V	Digital supply voltage		1.8		Note2
Gate Driver High voltage	VGH	V		10.0		16.0	Note3
Gate Driver Low voltage	VGL	V		-16.0		-7.5	Note3
Driver Supply voltage		V	VGH-VGL	19		32	Note3
<b>Input/Output</b>							
Logic High level input voltage	VIH	V		0.7VDDI		VDDI	Note1,2,3
Logic Low level input voltage	VIL	V		VSS		0.3VDDI	Note1,2,3
Logic High level output voltage	VOH	V	IOH = -1.0mA	0.8VDDI		VDDI	Note1,2,3
Logic High level output voltage	VOL	V	IOL = 1.0mA	VSS		0.2VDDI	Note1,2,3
Logic High level input current	IIH	μA				1	Note1,2,3
Logic Low level input current	IIL	μA		-1			Note1,2,3
Logic input leakage	IIL	μA	VIN = VDDI or VSS	-0.1		+0.1	Note1,2,3

current							
<b>VCOM Operation</b>							
VCOM High voltage	VCOMH	V	Ccom=12nF	2.5		5.0	Note 3
VCOM Low voltage	VCOML	V	Ccom=12nF	-2.5		0.0	Note 3
VCOM Amplitude voltage	VOMA	V	VCOMH-VCOML	4.0		5.5	Note 3
<b>Source Driver</b>							
Source output range	Vsout	V		0.1		AVDD-0.1	Note4
Gamma reference voltage	GVDD	V		3.0		5.0	Note3
Source output setting time	Tr	μS	Below with 99% precision		15	20	Note4,5
Output deviation voltage (Source output channel)	Vdev	mV	Sout >= 4.2V			20	Note4
		mV	Sout <=0.8V			15	-
Output offset voltage	VOFSET	mV				35	Note6
<b>Booster Operation</b>							
1 <sup>st</sup> Booster (VPNLx2) voltage	AVDD	V		4.5*6		6*7	Note3
1 <sup>st</sup> Booster(VPNLx2) Drop voltage	VPNLx2, drop	%	I loading = 1mA			5	Note3
Liner range	VLinear	V		0.2		AVDD-0.2	

Note 1: VDDI=1.65 to 3.3V, VPNL=2.5 to 4.8V, AGND=GND=0V, Ta=-30 to 70°C (to +85°C no damage)

Note2: Please supply digital VDDI voltage equal or less than analog VPNL voltage. ( $VDDI \leq VPNL$ )

Note2,3,4: When the measurements are performed with LCD module. Measurement Points are like below.

Note3: CSX, RDX, WRX, D[23:0], D/CX, RESX, TE, PCLK, VS, HS, DE, SDA, SCL, GM2, GM1, GM0, RCM1, RCM0, P68, IM2, IM1, IM0, SRGB, REV, SMX, SMY, RL, TB, IDM, SHUT, PREG, GS and Test pins.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

Note6: The Max. value is between with Note 4 measure point and Gamma setting value.



	trdh	Control pulse H duration(ID)	90		ns	data
	trdl	Control pulse L duration(ID)	45		ns	
RDX	trcfm	Read cycle (FM)	450		ns	When read from frame memory
	trdhfm	Control pulse H duration (FM)	90		ns	
	trdlfm	Control pulse L duration (FM)	355		ns	
D[17..0]	tdst	Data setup time	10		ns	For maximum CL = 30pF For minimum CL = 8pF
	tdht	Data hold time	10		ns	
	trat	Read access time (ID)		40	ns	
	tratfm	Read access time (FM)		340	ns	
	todh	Output disable time	20	80	ns	

Note 1: VDDI 1.65 to 3.3V, VPNL=2.6 to 3.3V, AGND=GND=0V, Ta=-30 to 70 °C (to +85°C no damage)

Note 2: This input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals

## 17.3.2. Display Serial Interface (SPI)

### 17.3.2.1 3-pin Serial Interface

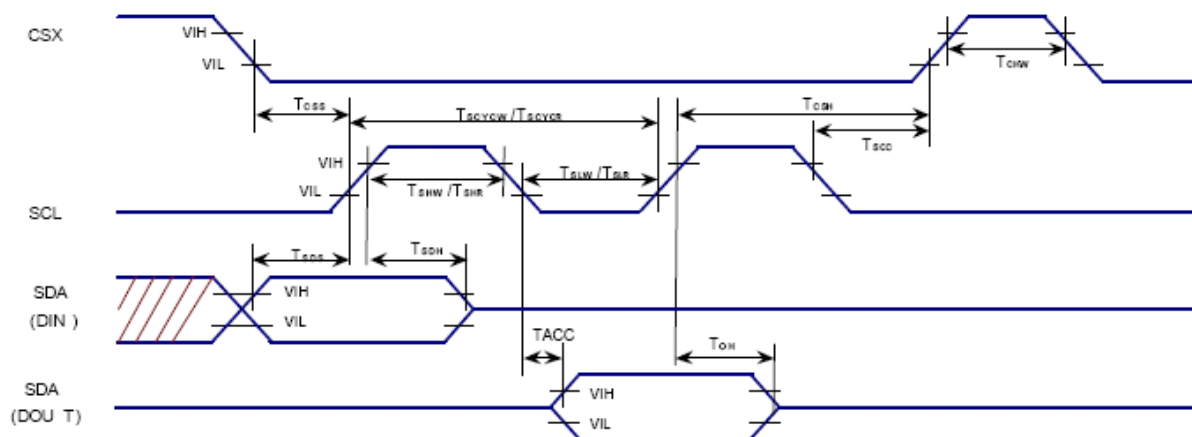


Table 17.3.2.1: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T <sub>CSS</sub>	Chip select setup time	10		ns	
	T <sub>CSH</sub>	Chip select hold time	30		ns	
	T <sub>CHW</sub>	Chip select "H" pulse width	30		ns	
SCL	T <sub>SCYCW</sub>	Serial clock cycle(Write)	33		ns	
	T <sub>SHW</sub>	S"L""H" pulse width(Write)	10		ns	
	T <sub>SLW</sub>	S"L""L" pulse width(Write)	10		ns	
	T <sub>SCYCR</sub>	Serial clock cycle(Read)	100		ns	
	T <sub>SHR</sub>	S"L""H" pulse width(Read)	40		ns	
	T <sub>SLR</sub>	S"L""L" pulse width(Read)	40		ns	
SDA(DIN) (DOU T)	T <sub>SDS</sub>	Data setup time	5		ns	
	T <sub>SDH</sub>	Data hold time	5		ns	
	T <sub>ACC</sub>	Access time	5	25	ns	For maximum CL = 30pF
	T <sub>OH</sub>	Output disable time	10		ns	For minimum CL = 8pF

Note 1: VDDI=1.65 to 3.3V, VPNL=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70°C (to +85°C no damage)

Note 2 : The input signal rise time and fall time(tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 10% and 90% of VDDI for Input signals.

### 17.3.2.2 4-pin Serial Interface

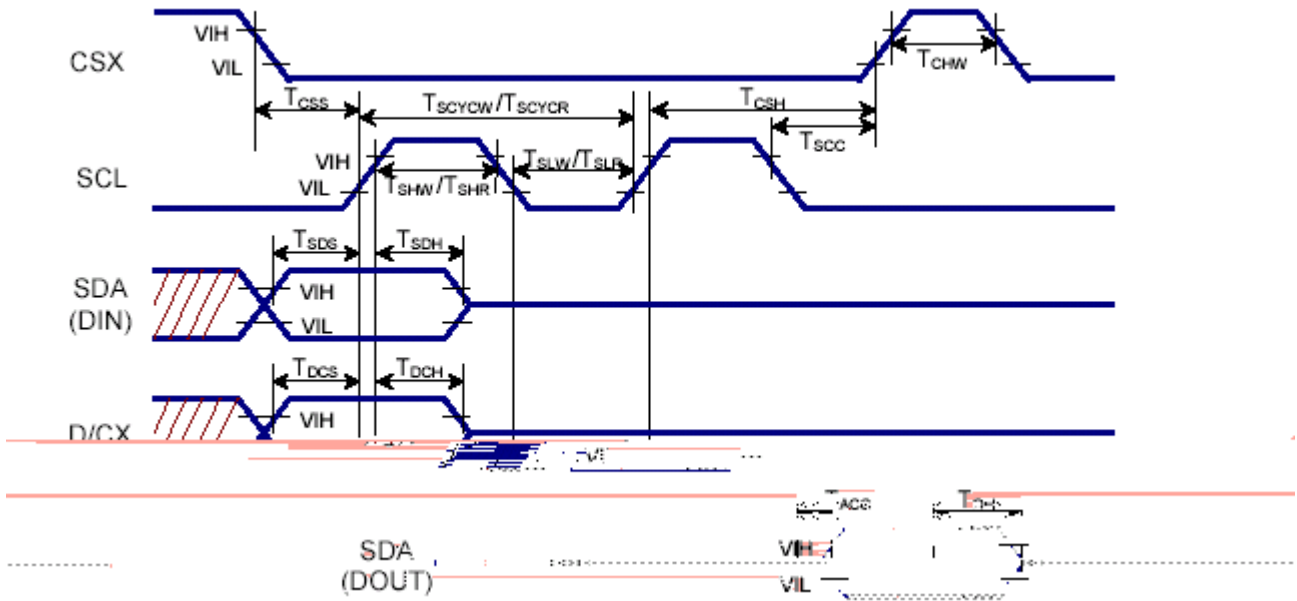


Table 17.3.2.2: 4 pin Serial Interface Characteristics

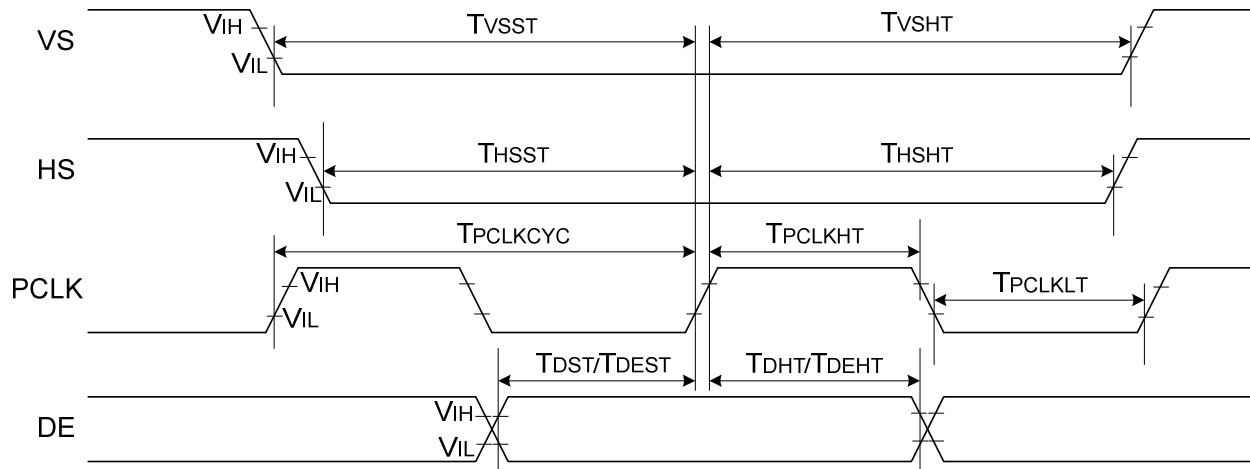
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	10		ns	
	TCSH	Chip select hold time	30		ns	
	TCHW	Chip select "H" pulse width	30		ns	
SCL	TSCYCW	Serial clock cycle(Write)	33		ns	
	TSHW	S"L""H" pulse width(Write)	10		ns	
	TSLW	S"L""L" pulse width(Write)	10		ns	
	TSCYCR	Serial clock cycle(Read)	100		ns	
	TSHR	S"L""H" pulse width(Read)	40		ns	
	TSLR	S"L""L" pulse width(Read)	40		ns	
D/CX	TDCS	D/CX setup time	5		ns	
	TDCH	D/CX hold time	5		ns	
SDA(DIN) (DOUT)	TSDS	Data setup time	5		ns	
	TSDH	Data hold time	5		ns	
	TACC	Access time	5	25	ns	For maximum CL = 30pF
	TOH	Output disable time	10		ns	For minimum CL = 8pF

Note 1: VDDI=1.65 to 3.3V, VPNL=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70°C (to +85°C no damage)

Note 2 : The input signal rise time and fall time(tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 10% and 90% of VDDI for Input signals.

### 17.3.3. Parallel RGB 18/16/6-bit Bus



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
PCLK	TPCLKCYC	Pixel low pulse width	15	-	ns	
	TPCLKHT	Pixel high pulse width	15	-	ns	
VS	TVSST	Vertical Sync. setup time	15	-	ns	
	TVSHT	Vertical Sync. hold time	15	-	ns	
HS	THSST	Horizontal Sync. setup time	15	-	ns	
	THSHT	Horizontal Sync. hold time	15	-	ns	
DE	TDEST	Data Enable setup time	15	-	ns	
	TDEHT	Data Enable hold time	15	-	ns	
D[17:0]	TDST	Data setup time	15	-	ns	
	TDHT	Data hold time	15	-	ns	



**18.Revision History**

Version No.	Date	Page	Description
V.01	2009/12/28		New Created