

Watchdog Timer:	Disabled
PLL Prescaler Selection bits:	Divide by 3 (12 MHz oscillator input)
Stack Overflow/Underflow Reset:	Enabled
Extended Instruction Set:	Disabled
Background Debug:	Disabled
CPU System Clock Postscaler:	No CPU system clock divide
Code Protect:	Enabled
Config Word Signature Bit:	Bulk erase of memory not conducted
RESERVED:	RESERVED
Oscillator:	HS+PLL, USB-HS+PLL
T1OSCEN Enforcement:	Enabled
Low-Power Timer1 Oscillator:	Disabled
Fail-Safe Clock Monitor:	Disabled
External Oscillator Switch Over Mode:	Disabled
Watchdog Postscaler:	1:32768
RESERVED:	RESERVED
DSWDT Clock Select:	DSWDT uses INTRC